NEW TECHNICAL THEORY FOR SERVICING

LVS-5000/6000P

OPERATION MANUAL

Laser Videodisc Recorder

SONY®

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1. EN-4 BOARD

The circuit functions of the EN-4 board include: internal Ref SYNC, various clamp sampling pulse generation, color different input, Y/C separation and decoding of composite video signals, playback amplifier, Y-R/B → RGB conversion, and RGB → Y-R/B conversion.

The composite video signal undergoes Y/C separation by the 3-line tandem filter which comprises the vertical correlation circuit and the horizontal correlation circuit. The vertical correlation circuit separates the chroma (c) signal from the composite video signal. The horizontal correlation signal eliminates the Y signal component remaining in the separated chroma signal and separates the Y signal and the C signal.

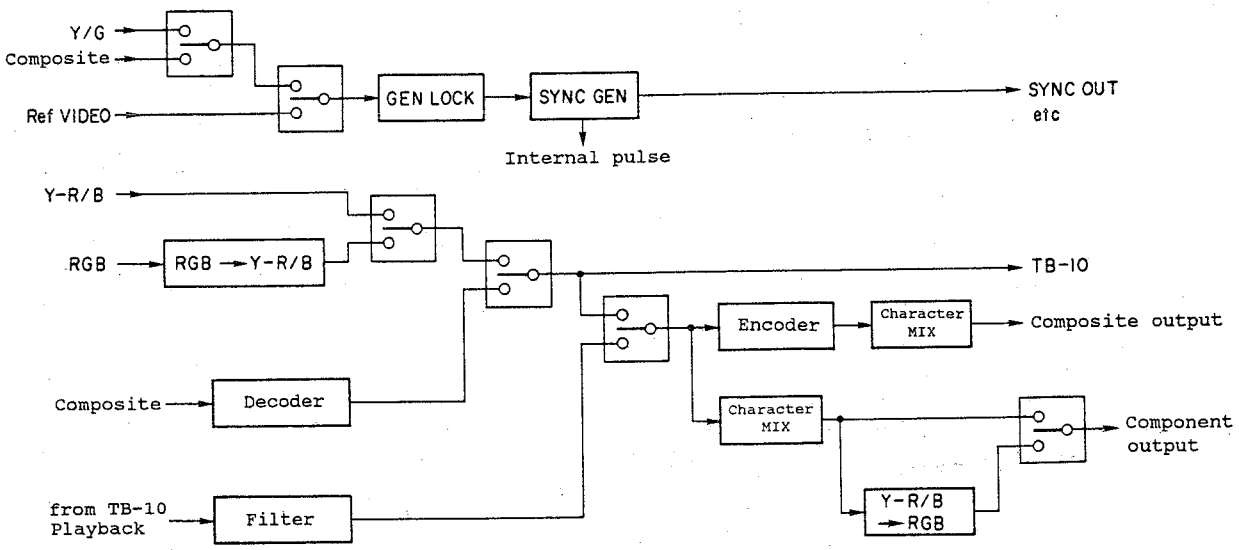


Fig. 1-1

1-1 SYNC GENERATION BLOCK

1-1-1 SYNC SEPARATION AND BURST SEPARATION CIRCUITS

As a synchronizing signal, the input signal corresponding to each input mode becomes Ref. However, when Ref VIDEO is input to the Ref VIDEO terminal, the input signal is forced to changeover to Ref VIDEO.

Also, to stabilize the internal SYNC during blank search, the external signal is muted.

The hybrid IC separates the synchronization and burst.

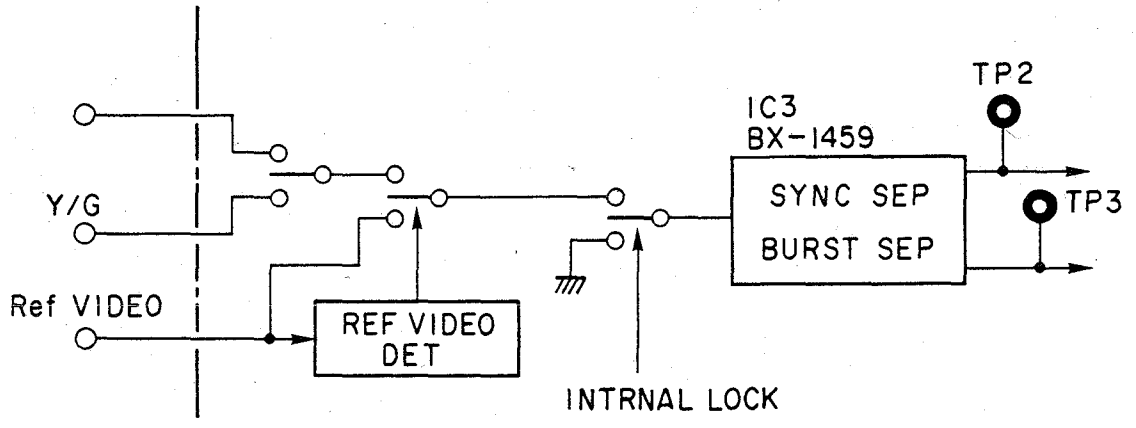


Fig. 1-2

1-1-2 GENLOCK DRIVE AND SYNC SIGNAL GENERATION CIRCUITS

IC4 is a genlock drive circuit, and IC6 is a synchronizing signal generation circuit. The signal which passes through the synchronized separation circuit and the burst separation circuit is input to the phase comparison circuit IC4. The synchronizing signal that is input to pin (17) and the HD signal that is input to pin (15) are compared. Then they are output from pin (9) as the H COM OUT signal. Also, the EXT SC signal that is input to pin (4) and the INT SC signal that is input to pin (18) are output as the SC COM OUT signal from pin (1). VCO1 (X1) and VCO2 (X2) use these signals to send each standard frequency to IC6, which is the synchronizing signal generation circuit. Since the standard frequency is 910 fH (4 fsc) during the NTSC mode, VCO1 operation is prohibited during the INT mode. Q6 and Q7 operate as VCO1's switchers. During the INT mode, they terminate VCO1's functions. IC6 can output various signals that have undergone genlock by VCO1 and VCO2.

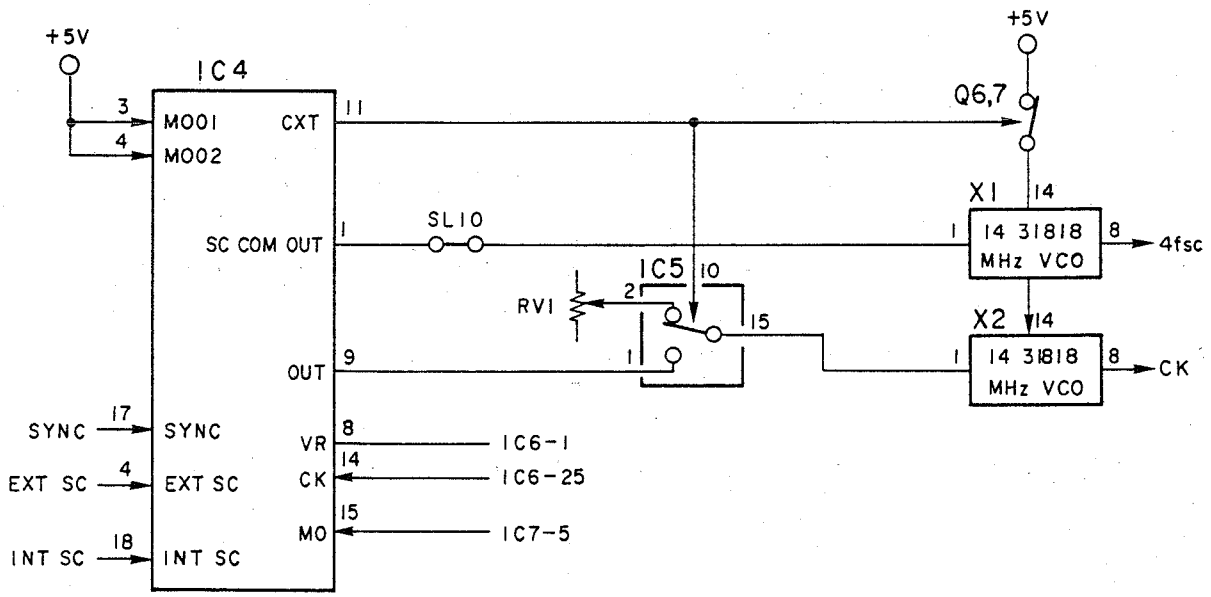


Fig. 1-3 Genlock drive and SYNC signal generation circuits

1-1-3 CLAMP PULSE AND SAMPLING PULSE GENERATION CIRCUITS

The clamp and sampling pulses used on the EN board are mainly generated with a monostable multivibrator using the SYNC, FLD, and BF signals output from the IC6 synchronization signal generation circuit.

Also, signals for off the EN board, for example TB-10, are output with a buffer that can be enabled or disabled. When PAL is selected, the output goes to high impedance and the connection is cut.

Also, signals for off the EN board, for example TB-10, are output with the enabled buffer. When PAL is selected, the output goes to high impedance and the connection is cut.

Major functions of signals:

(1) SYNC OUT : SYNC during PB
(2) OH SYNC : Spindle standard during PB
(3) NT REF SYNC : SYNC OUT signal
(4) H SYNC : Timing at SYSCON
: Standard for TBC PLL
(5) S REF : Standard for audio PCM IC
(6) V SYNC : Timing at SYSCON
(7) V LOAD : V reset for TBC

1-2 COMPOSITE BLOCK

1-2-1 VIDEO INPUT LEVEL CONTROL CIRCUIT

The input composite video signal activates the AGC with the video level controller IC111. The signal that is output from pin (12) of IC111 undergoes sample holding by IC114, and its SYNC chip level is adjusted by RV112. Then the signal is returned to IC111. IC111's output signal that has undergone AGC processing is output to TP112 after the direct current bias is controlled by RV111.

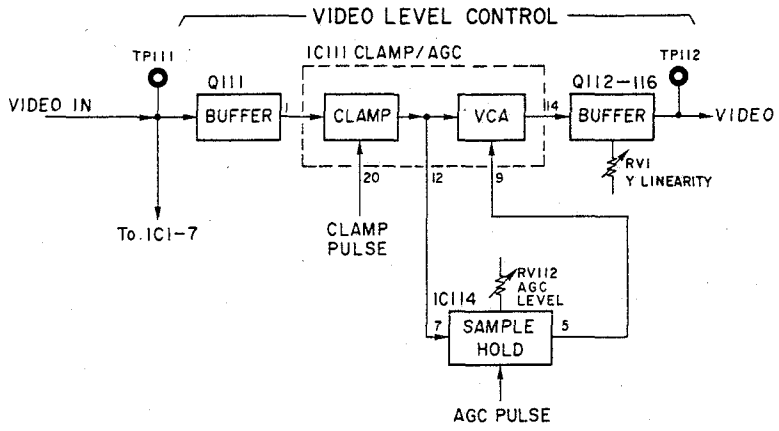


Fig. 1-4

The input during B/W also passes through this AGC.

1-2-2 1H/2H DELAYED VIDEO AGC LOOP

In order to enable Y/C separation, the signal that appears at TP112 is divided into two signals: a non-delayed signal and a 1H/2H delayed signal.

The 1H/2H delayed signal is input to the amplitude moderation circuit IC113. It undergoes amplitude modulation by a 30 MHz oscillator. The amplitude modulated signal passes through the glass-type 1H delayed line DL111 (1/2) and then it is amplified. Then the signal is output to TP116 as a 1H delayed signal. Also, the signal that has passed through the delayed line passes through another 1H delayed line DL111 (2/2) and then it is amplified. Then the signal is output to TP117 as a 2H delayed signal. The above non-delayed signal (TP115), the 1H delayed signal (TP116), and the 2H delayed signal (TP117) have their respective SYNC chips clamped by the SYNC signal that was separated from the composite signal. Also, the signal that clamped the SYNC chip undergoes sample holding by the burst gate pulse that was separated from the composite signal. IC118 compares these three signals, then the error components are returned to the 1H delayed signal and the 2H delayed signal. The AGC loop operates to keep the level constant for the non-delayed signal, the 1H delayed signal, and the 2H delayed signal.

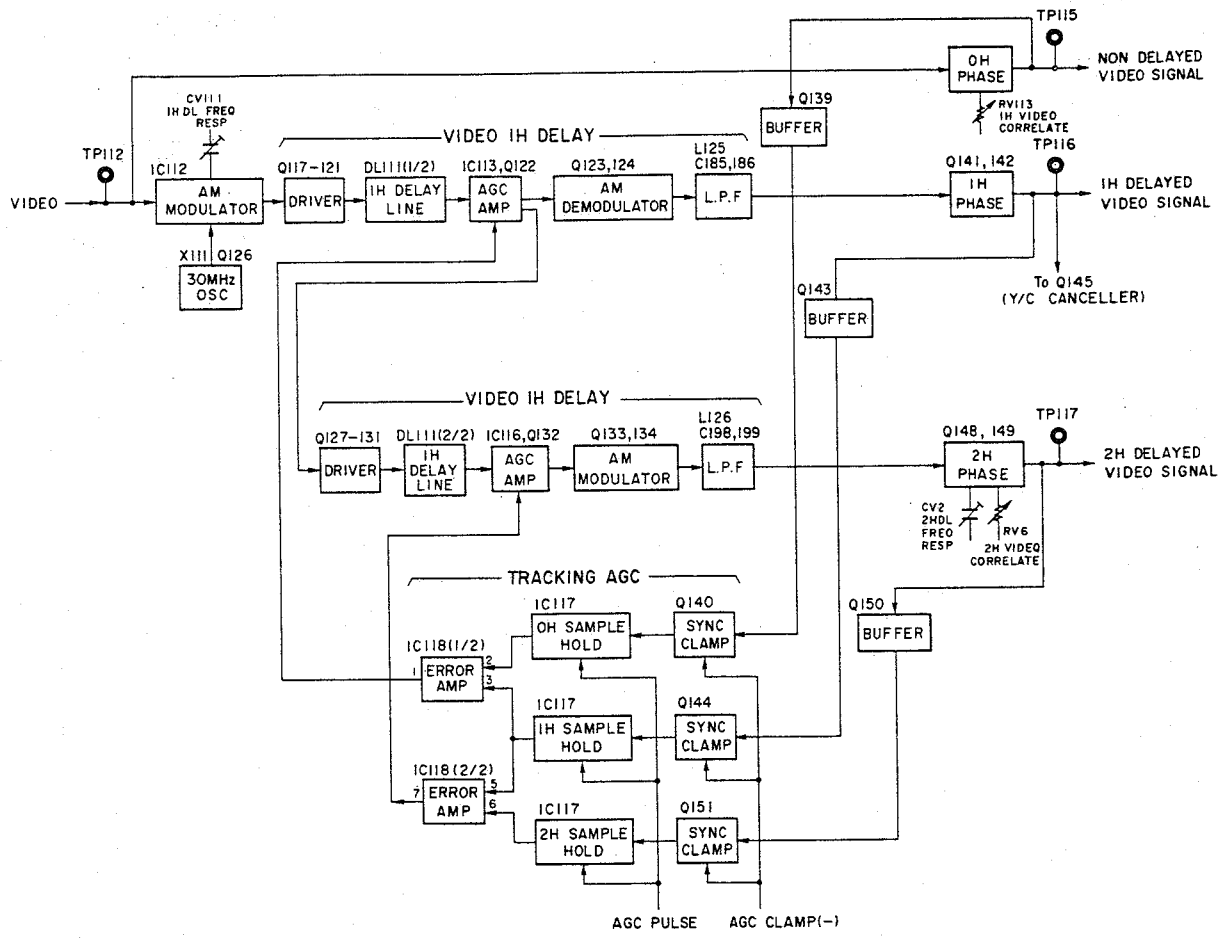


Fig. 1-5 1H/2H delayed video AGC loop

1-2-3 CHROMA SIGNAL CORRELATOR

The TP115, TP116, and TP117 signals are input to the correlation circuit's (IC254) internal vertical correlation circuit. The resulting output is delayed by 140 nsec and 280 nsec by delay line DL251. Then it is input to the horizontal correlation circuit along with the non-delayed signal from the vertical correlation circuit. The horizontal correlation circuit separates the Y signal component (which cannot be separated by the vertical correlation circuit) from the chroma signal and outputs the completely separated chroma signal to TP253. The 140 nsec delay by DL251 is equal to half a cycle of a sub carrier. And the 280 nsec delay is equal to 1 cycle. When the signal is processed by the horizontal correlation circuit, the Y signal component is eliminated along with the chroma signal's edge component. Thus, the horizontal correlation circuit's output signal is sent to the chroma edge compensation circuit IC255 to compensate for the edge component.

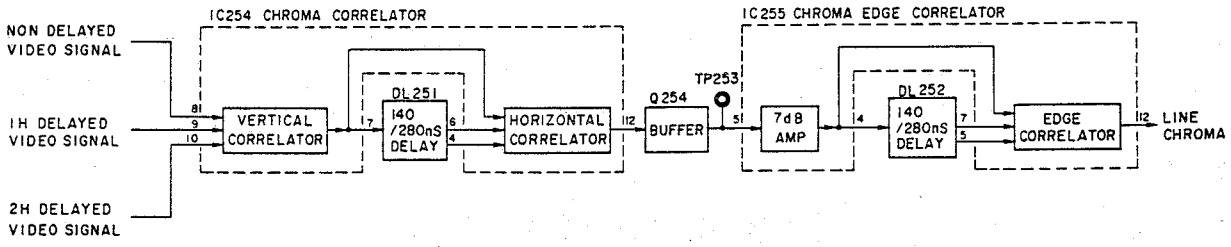


Fig. 1-6 Chroma signal correlation circuit

1-2-4 CHROMA PHASE LOCK LOOP

This circuit makes the line chroma's phase be 180° different from the phase of the chroma on the main line video at the mix point where Y/C is cancelled. The main line video passes through from TP116 to the 350 ns delay line. Therefore, when TP116 is set as the standard, the chroma's phase will be:

$$350\ \text{ns} / 280\ \text{ns} \times 360 = 360 + 90$$

(280 ns: Chroma period)

The phase is therefore 90°. This makes it necessary for the line chroma's phase to be 270°. When the line chroma passes through IC254,255 it is delayed by about 180 ns with respect to TP116. So in order to have a 270° phase, another delay of about 30 ns is necessary. This delay is produced by the L266 circuit and variable capacitors D251 and D252. The variable capacitor's bias is controlled so that the line chroma output has a constant 270° phase difference with respect to TP116.

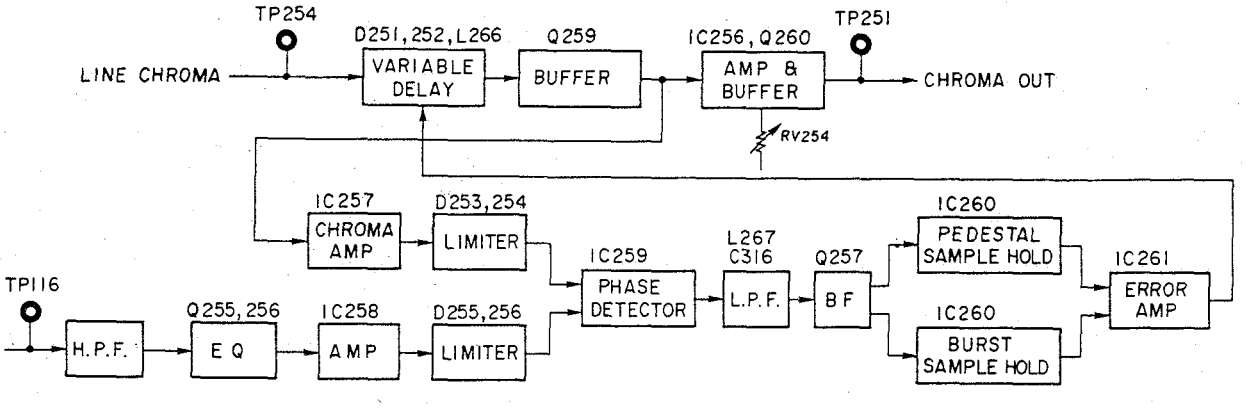


Fig. 1-7 Chroma phase lock circuit

1-2-5 Y/C CANCEL CIRCUIT

This circuit is input with the chroma signal from the 1H delayed video signal which appears at TP116 and from the edge compensation circuit. Q261 eliminates the chroma signal from the 1H delayed signal and extracts the Y signal.

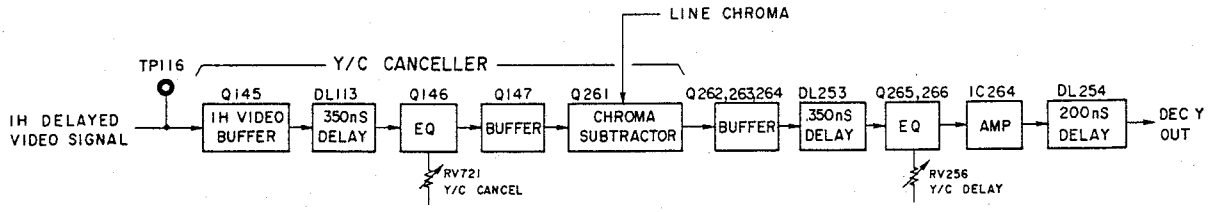


Fig. 1-8 Y/C cancel circuit

1-2-6 CHROMA (B-Y/R-Y) DECODER

The chroma signal, which underwent Y/C separation from the composite video signal through Y/C separation, is input. A 3.50 MHz carrier is input to the B-Y decoder IC351, then the decoded B-Y signal is output. The 3.58 MHz carrier component of this B-Y signal is eliminated by the FL351 low-pass filter. With Q357, the SYNC chip is clamped to 0V. The blanking level is adjusted, then the signal appears at TP352. Meanwhile, the 3.58 MHz carrier having a 90° phase difference is input to the R-Y decoder IC352, and the decoded R-Y signal is output. This R-Y signal also undergoes the same signal processing as the above B-Y signal and appears at TP353.

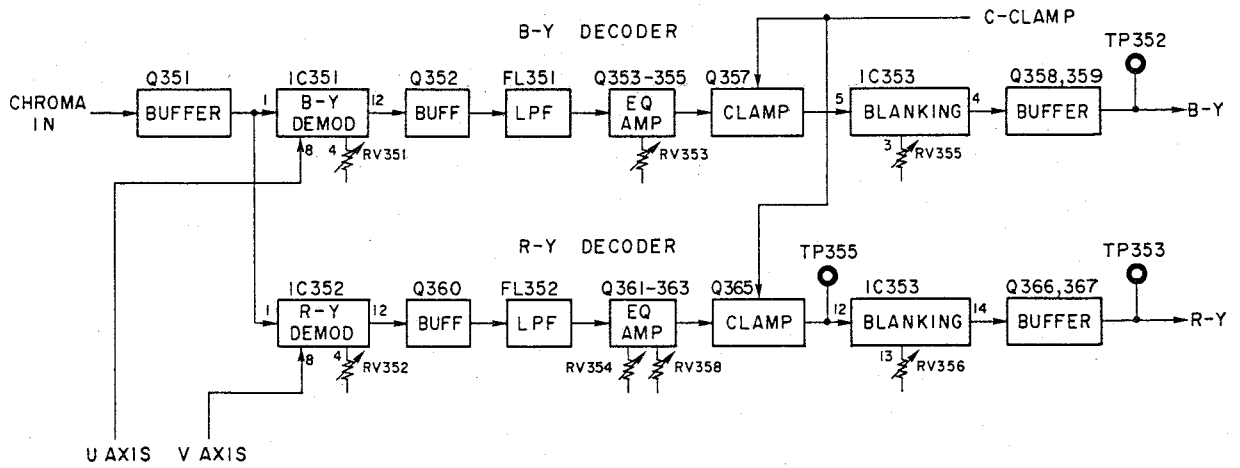


Fig. 1-9 B-Y/R-Y decoder

1-2-7 U/V AXIS SIGNAL GENERATION CIRCUIT

The 3.58 MHz carrier which is used as a chroma decoder is generated as follows. TP355's R-Y signal is input to IC354, and only the burst portion is extracted from the R-Y signal by the burst gate pulse which is input to pin (10) of IC353. The extracted burst signal is held by the capacitor. The direct current voltage that is held passes through IC354, then it is input to the oscillator circuit of VCO. VCO's oscillation output is divided into four by IC365. The 4 subcarriers pass through IC357 (1/2), then they are sent to the R-Y decoder IC352 as a V axis signal. In addition, the four subcarriers are delayed by 1 clock by IC357 (2/2). The phase is shifted 90° and they are input to the B-Y decoder IC351 as a U axis signal.

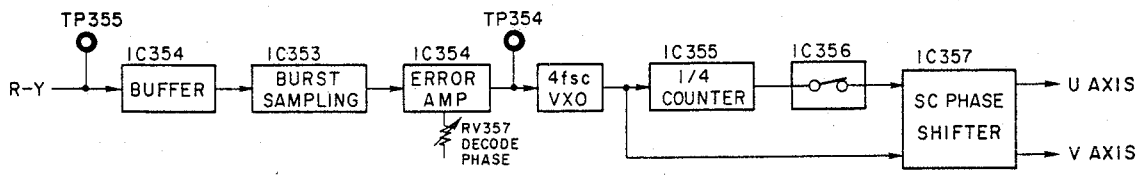


Fig. 1-10 U/V axis signal generation circuit

1-3 SIGNAL SELECTION BLOCK

1-3-1 R-Y/B-Y SELECT CIRCUIT

TP352's decoded B-Y signal and TP353's decoded R-Y signal are respectively input to the B-Y select circuit and the R-Y select circuit. Since the B-Y select circuit. Since the B-Y select circuit and the R-Y select circuit have the same circuit configuration, only the R-Y select circuit will be described here.

Of the three types of signals (the signal which was turned into -Y after the matrix processing of the R-Y signal that was input to the connector panel's R-Y/R IN connector and after the matrix processing of the R signal that was input to the connector panel's R-Y/R IN connector, the composite signal that was input to the connector panel's COMPOSITE1 B/W IN, and the decoded R-Y signal), one is selected by IC52's switcher. The selected signal is divided into 2 signals. After passing through CN102 4A, one signal is sent to the TB-10 board, and the other signal becomes the EE system's signal.

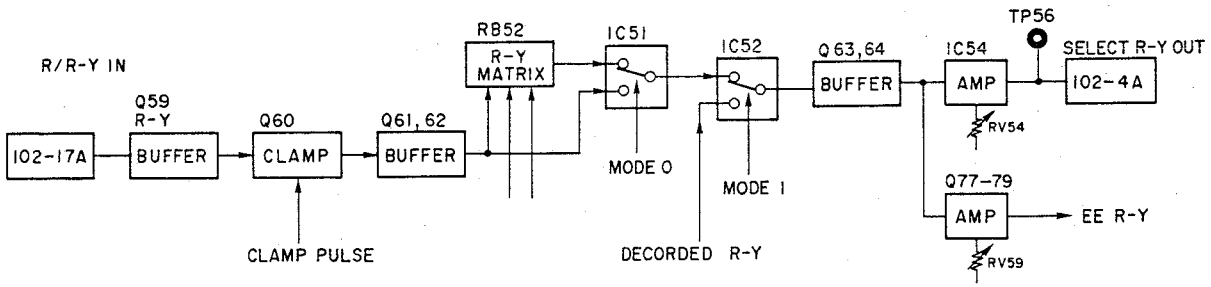


Fig.1-11 R-Y selector

1-3-2 Y-SIGNAL SELECT CIRCUIT

One of the following three signals is selected by IC52's switcher: the Y signal that is input to the connector panel's G/Y IN connector, the G signal that is input to the connector panel's G/Y connector and becomes Y by the matrix circuit, and the Y signal that underwent Y/C separation from the composite signal that was input to the connector panel's COMPOSITE 1 B/W IN connector. The selected signal is divided into two signals. One signal passes through CN102 2A, then it is sent to the TB-10 board. The other signal becomes the EE system's signal.

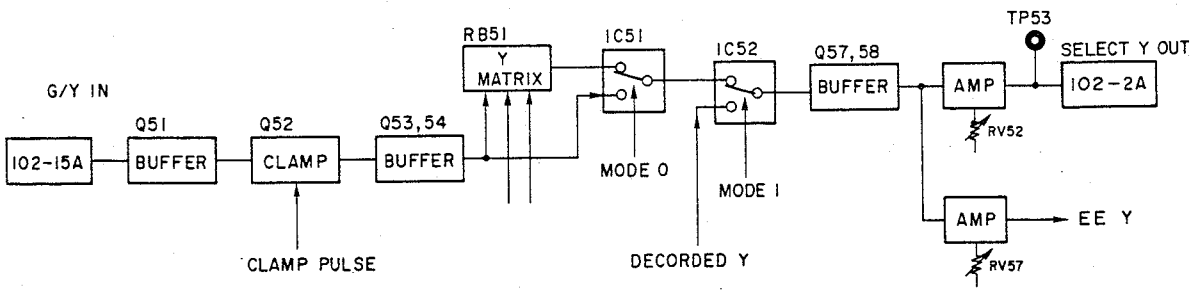


Fig. 1-12 Y selector

1-4 PLAYBACK BLOCK

1-4-1 CHROMA CLAMP CIRCUIT

The expanded B-Y signal from the TB-10 board passes through LPF, and the TBC's clock noise is eliminated. After passing through IC441 AMP, the signal is input to the IC443 switcher. This switcher changes over PB and EE. The B-Y signal which passes through the switcher is clamped by Q443. Also, the blanking level is adjusted by IC444, and the signal is output as a clamped B-Y signal and input to the next step's chroma encoder circuit. The R-Y signal is also processed by the circuit in the same way.

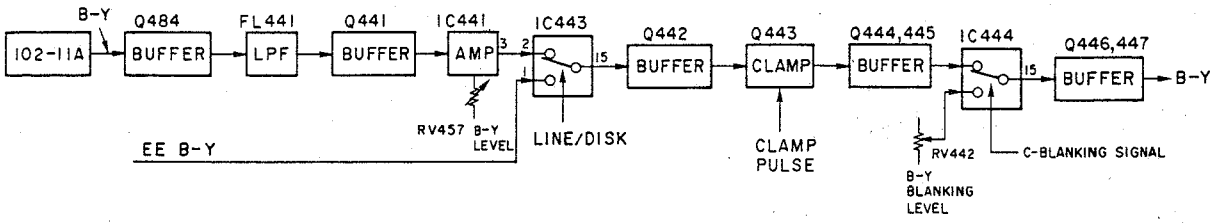


Fig. 1-13 Chroma clamp circuit

1-4-2 Y CLAMP AND STANDARD SYNC ADDED CIRCUITS

Having a compensated time axis that is input from the TB-10 board, the Y signal's TBC clock noise is eliminated by the low-pass filter. The signal then passes through IC449 AMP, and it is input to the IC443 switcher. This switcher changes over PB and EE. The Y signal which passes through the switcher is clamped by Q465 and added with the SYNC signal by IC451.

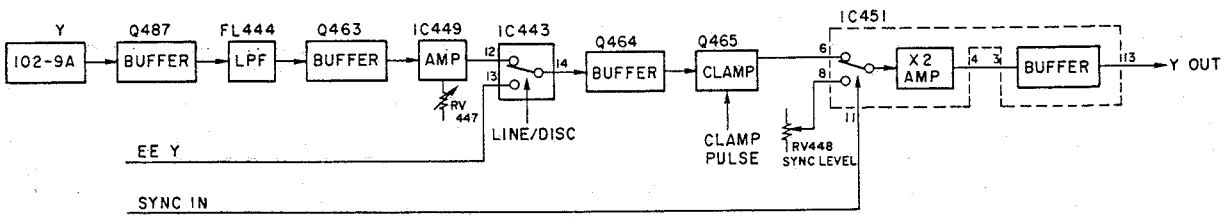


Fig. 1-14 Y clamp and standard SYNC added circuits

1-5 COMPOSITE ENCODER

1-5-1 CHROMA ENCODER

The clamped B-Y signal is input to IC446. The B-Y signal is encoded to a composite signal by the subcarrier. Also, the R-Y signal undergoes the same signal processing for encoding. The encoded signal is mixed in IC446 and output from pin (8) of IC446. This signal passes through a 3.58 MHz band-pass filter, and it is output as a composite chroma signal.

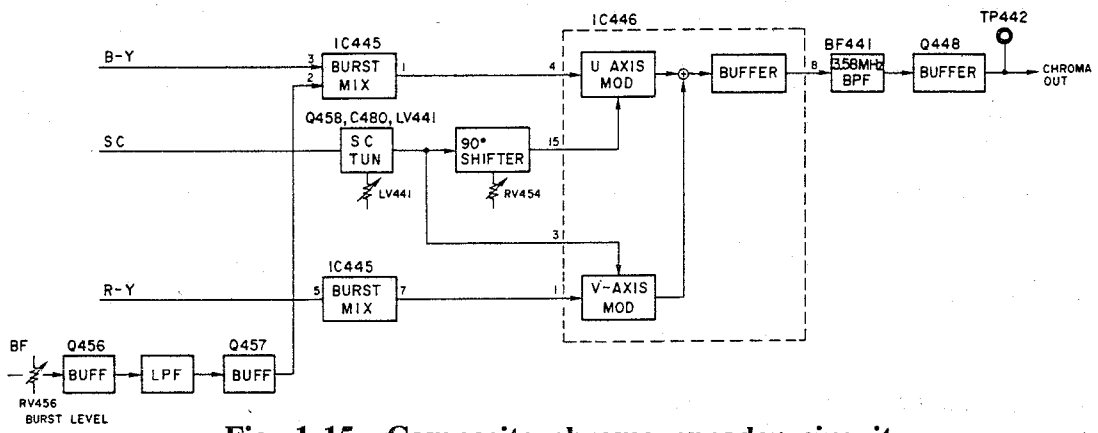


Fig. 1-15 Composite chroma encoder circuit

1-5-2 COMPOSITE VIDEO SIGNAL PROCESSING

The Y signal that is output from pin (4) of IC451 is delayed by DL441, and it is sent to the chroma signal mixing circuit which comprises Q470 and Q471. This chroma signal is a composite chroma signal that was generated by the chroma encoder. The signal mixed with the chroma signal becomes a composite video signal which is sent to the IC456 switcher. IC456 changes over the composite signal and the B/W signal. Also, the IC563's switcher switches the BYPASS VIDEO (AGC VIDEO). The composite video signal that passes through IC456 and IC563 is sent to the character mix circuit and output to CN102 23A.

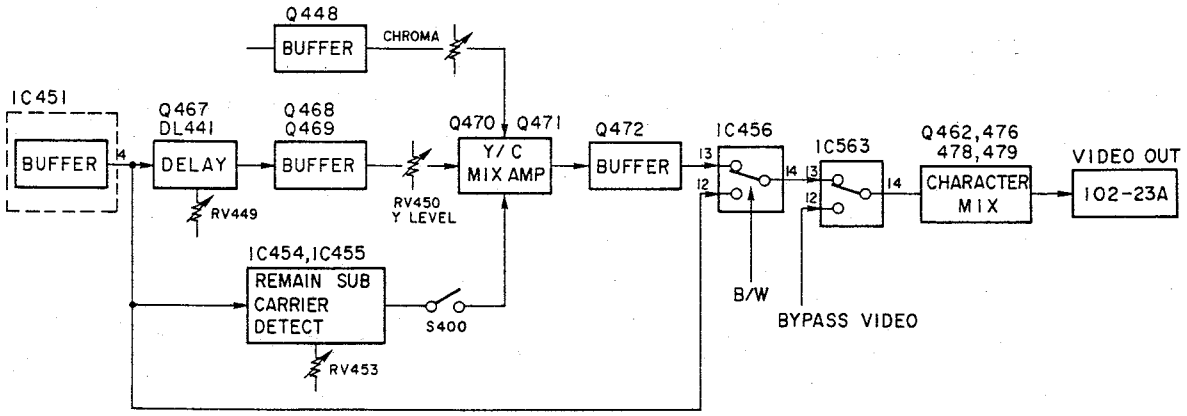


Fig. 1-16 Composite video signal processing

1-6 COMPONENT OUTPUT BLOCK

1-6-1 COMPONENT SYSTEM Y-SIGNAL

The Y signal that is output from pin (13) of IC451 is sent to the character mix circuit. Then in the next step, the SYNC portion is muted by IC563, and the signal is sent to IC563 (2/3). IC563 (2/3) decides whether to mute the SYNC portion. The Y signal that passes through IC563 is supplied to the G matrix circuit where it undergoes Y → G conversion. IC562 is a switcher which selects Y or G. IC565 selects the Y signal while in the B & W mode. The signal that passes through Q568 is output to CN102-20A.

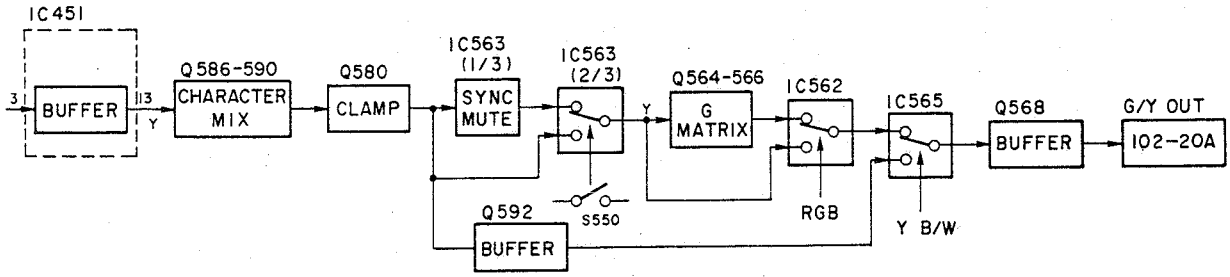


Fig. 1-17 Component Y

1-6-2 CHARACTER MIX CIRCUIT

The video signal that is input to Q462 undergoes SYNBC TIP CLAMP BY Q480. And after it passes through the Q476 buffer, Q477 attenuates the character insert portion's background to 1/2 level. Also, the character is mixed by Q479.

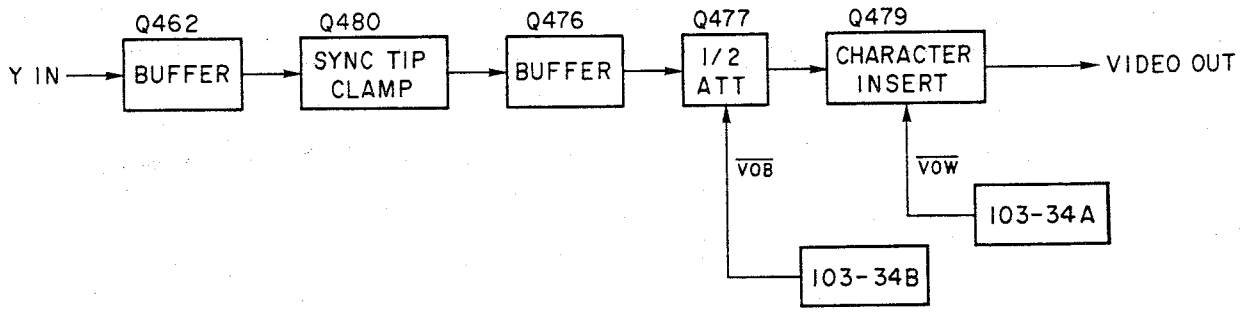


Fig. 1-18 Character mix circuit

1-6-3 COMPONENT SYSTEM CHROMA SIGNAL

The B-Y signal that passes through the clamp circuit is sent from the Q447 buffer to the RGB matrix circuit. The signal that underwent B-Y → B conversion is sent to IC562. IC562 selects B-Y or B. Also, the signal passes through IC565 and IC564, then it is output from CN102 21A. In the B & W mode, IC565 supplies the Y signal to the B channel.

In the B & W mode and in the Y, R-Y, B-Y output modes, IC564 mutes the B channel.

The R-Y signal is also processed in the same way by the circuit.

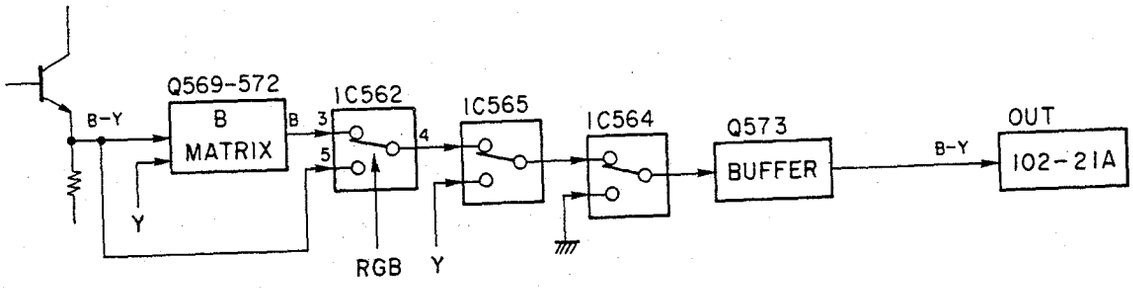


Fig. 1-19 Component chroma system

2. EP-9 BOARD

2-1 VIDEO INPUT LEVEL CONTROL CIRCUIT

AGC is applied to the input composite video signal, by video level controller IC111. The signal that is output through pin (12) of IC111 is sample-held by IC114, its sync chip level is adjusted by RV112, and then it is fed back to IC111. The output signal of IC111 that has undergone AGC processing is output to TP112.

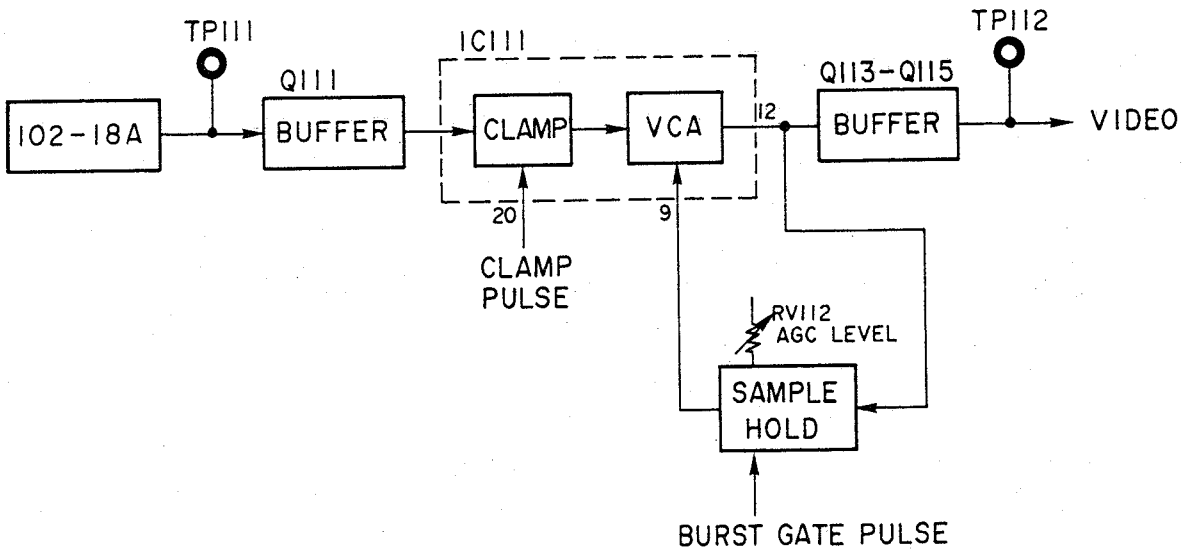


Fig. 2-1 Video input level control circuit

2-2 CHROMA SIGNAL CORRELATOR

Chroma component of the signal of TP112 is separated by a high-pass filter which is composed of R133, C130, R131, & R132. The signal is then input to an internal vertical correlation circuit, via pins (8) , (9) , (10) of IC115, its output is then delayed by 113 nsec to 226 nsec by delay line DL111, and finally it is input, together with the undelayed signal coming from vertical correlation circuit, into a horizontal correlation circuit. The horizontal correlation circuit separates the Y-signal component, which could not be separated by the vertical correlation circuit, from chroma signal; and outputs the totally separated chroma signal to TP114. The 113 nsec delay caused by DL111 is equivalent to half cycle of subcarrier, the 226 nsec delay is equivalent to 1 cycle. And, once the signal is processed by horizontal correlation circuit, both the Y-signal comment and edge

component of chroma signal is eliminated; therefore the output signal of horizontal correlation circuit is sent to chroma edge compensation circuit IC116, for the purpose of compensating its edge component.

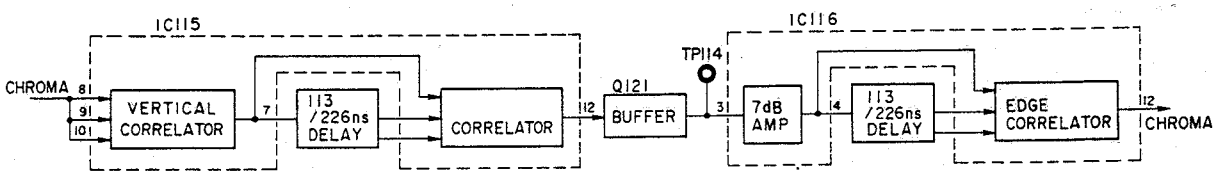


Fig. 2-2 Chroma signal correlat circuit

2-3 Y/C SEPARATION

To this circuit is input the video signal that appears in TP112. Chroma signal is eliminated from it by LPF, and Y-signal is extracted.

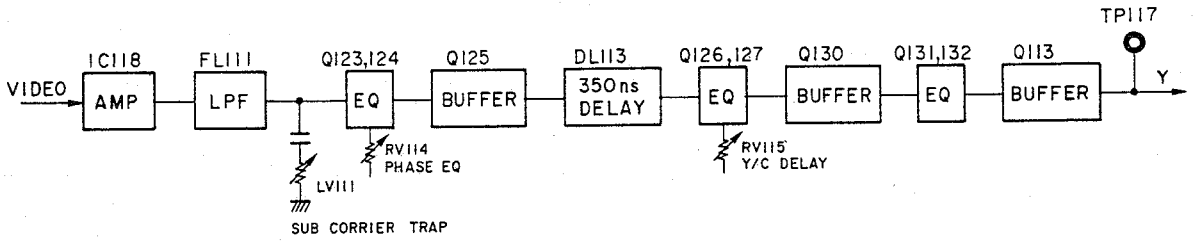


Fig. 2-3 Y/C separation circuit

2-4 CHROMA (B-Y/R-Y) DECODER

The chroma signal obtained by Y/C separation from composite video signal is input to this circuit. 4.33 MHz carrier is input into B-Y decoder IC351, and the decoded B-Y signal is output from it. The carrier component of 4.43 MHz is eliminated from this B-Y signal by low-pass filter FL351, sync chip is clamped to OR by Q351, blanking level is further adjusted, and the result appears in TP352. On the other hand, 4.43 MHz carrier, whose phase changes by ± 90° every 1H, is input into R-Y decoder IC352, and the decoded R-Y signal is output from it. This R-Y signal also is processed in the same way at the above mentioned B-Y signal, and finally appears in TP353.

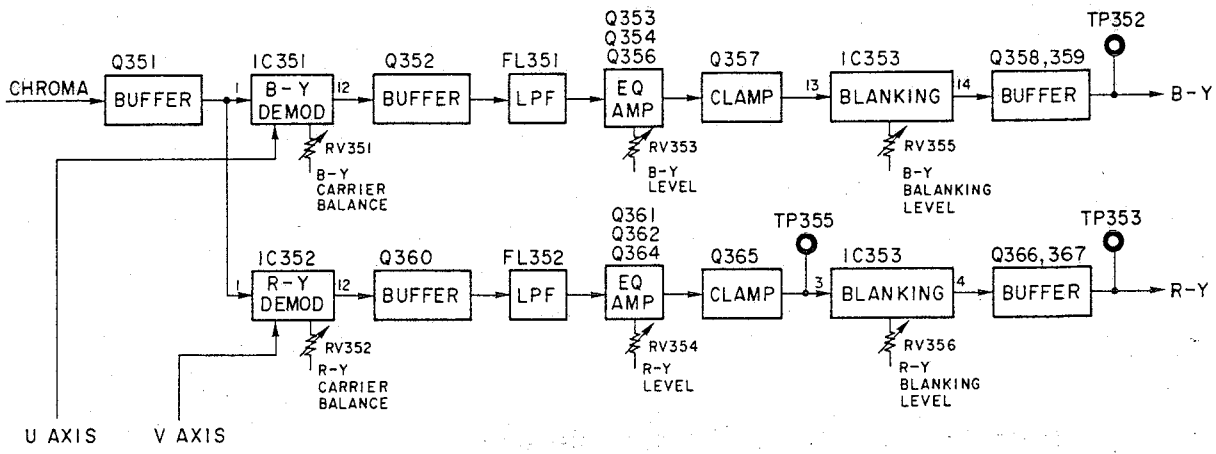


Fig. 2-4 B-Y/R-Y decoder

2-5 U/V AXIS SIGNAL GENERATION CIRCUIT

The 4.43 MHz carrier which is used by chroma decoder is generated in the following way. The R-Y signal of TP355 is input into IC360, and only the burst portion is extracted from it by burst gate pulse. The extracted burst signal is then half by a condenser, and the held DC voltage is input into generation circuit by VC0, and IC354. Oscillation output of VC0 is divided into 4 parts by IC355, this divided subcarrier passes through IC357, it is then inverted every 1H with LINE ALT signal, by IC361, and finally it is sent as V-axis signal to the earlier mentioned R-Y decoder IC352. Further the divided subcarrier is delated by 1 clock by IC357; that is, it is shifted through 90° , and finally it is sent as U-axis signal to the B-Y decoder IC351.

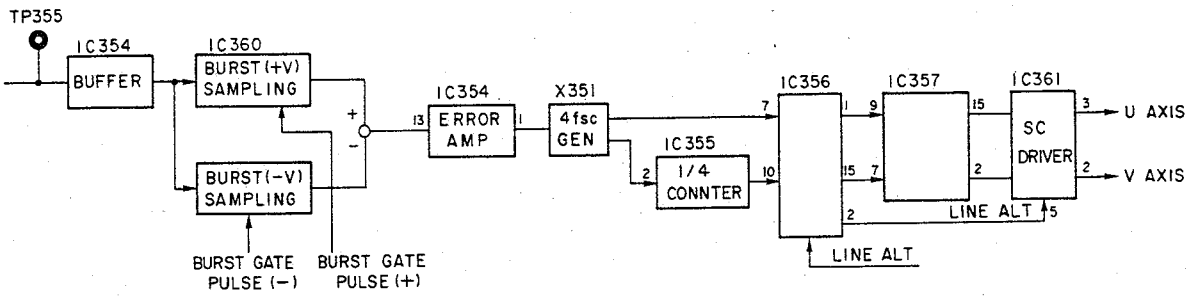


Fig. 2-5 U/V axis signal generation circuit

2-6 R-Y/B-Y SELECTION CIRCUIT

The B-Y and R-Y signals that are decoded by TP352 & TP353, are input into B-Y & B-Y selection circuits, respectively. Since, both B-Y & R-Y selection circuits are of identical configuration, only the R- selection circuit is discussed here.

One of the 3 different types of signals (R-Y signal that is input into R-Y/R, IN connector of connector panel; R-Y signal obtained by MATRIX processing the R signal that is input into R- /R, IN connector of connector panel; and R-Y signal obtained by decoding the composite signal that is input into COMPOSITE 7 B/W IN of connector panel) is selected by the switcher of IC52. The selected signal is then split up into 2 routes. One goes to TB-10 substrate via CN102 4A, and other goes to EE system.

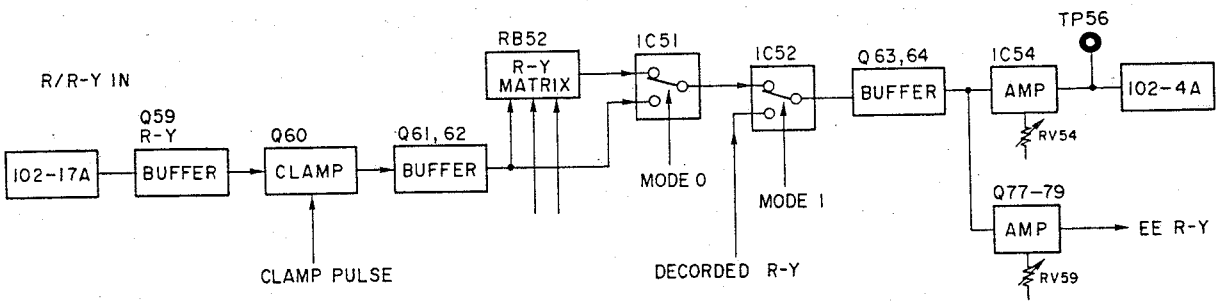


Fig. 2-6 R-Y selector

2-7 Y-SIGNAL SELECTION CIRCUIT

Y-signal selection circuit of the 3 different types of signals, that is, the Y-signal that in input into G/Y IN connector of connector panel, the Y-signal provided by MATRIX circuit by processing the G-signal that is input into G/Y connector of connector panel, and the Y/C separated Y-signal obtained from the composite signal that is input into COMPOSITE 7 B/W IN of connector panel, is selected by the switcher of IC52. The selected signal is then split up into 2 routes. One goes to TB-10 substrate via CN102 2A, and other goes to EE system.

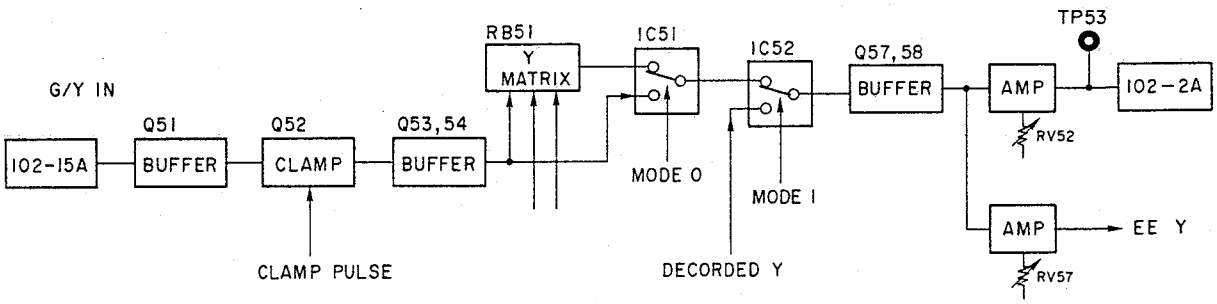


Fig. 2-7 Y selector

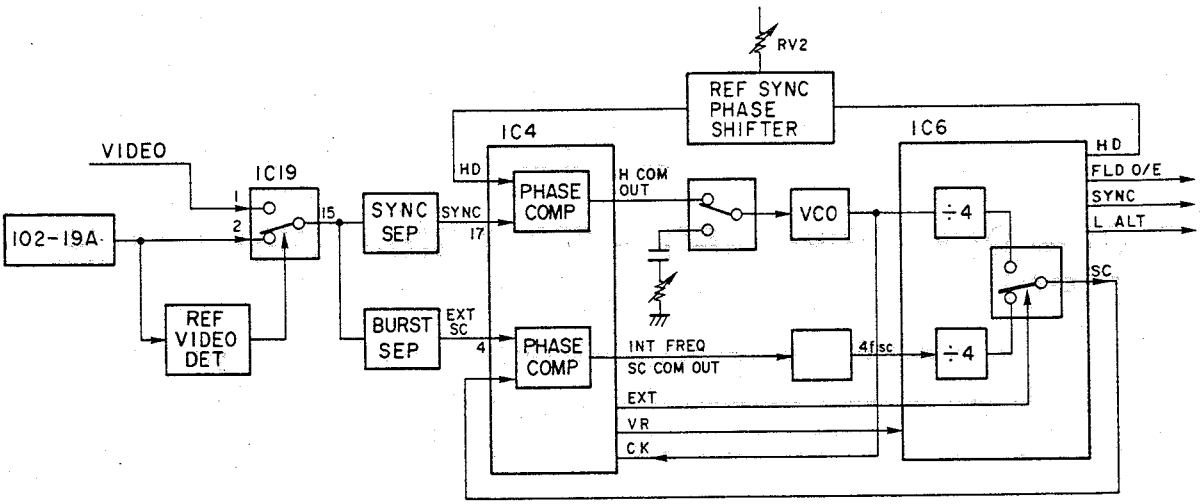


Fig. 2-8 GENLOCK circuit

2-8 SYNC SEPARATION AND BURST SEPARATION CIRCUITS

Synchronizing signal is detected, when REF VIDEO signal is input. Even if a signal is being input into COMPOSITE VIDEO 2 B/W IN terminal, the REF VIDEO IN terminal receives priority, provided a reference signal is being input into it also. The REF VIDEO signal that is selected by IC19 is divided into 2 routs, one leading to sync separation circuit and the other to burst separation circuit.

In the sync separation circuit, the subcarrier component is eliminated from it by a low-pass filter, and it is then input into sync chip clamp circuit by Q645. Sync chip level is clamped at 0V, it is then input into IC17 pin (4) , and the synchronizing signal is separated from it. In burst separation circuit, the signal is input into a burst filter that is composed of C648, L643, burst signal is separated from it by IC641, and the output of IC641 pin (7) is sent to IC4 pin (4) (EXT SC).

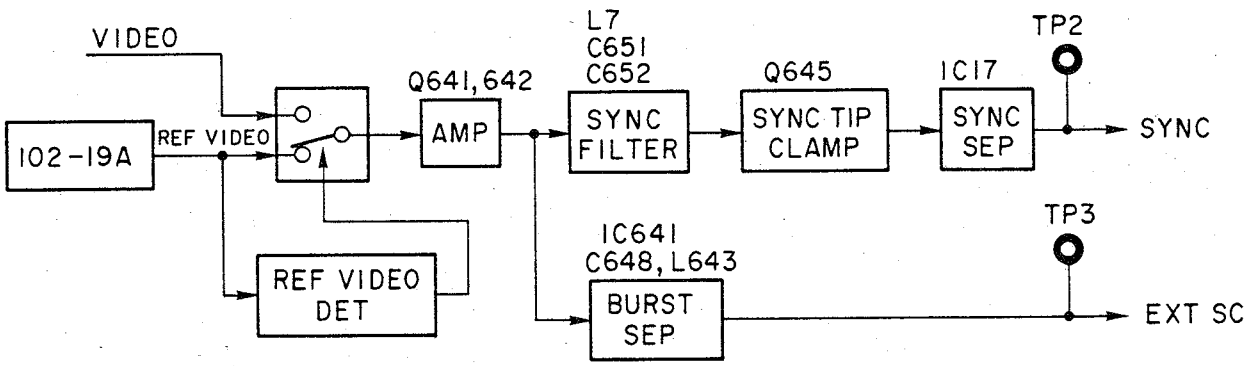


Fig. 2-9 SYNC separation and burst separation circuits

2-9 GENLOCK DRIVE AND SYNC SIGNAL GENERATION CIRCUITS

IC4 is the generation lock drive circuit, and IC6 is the synchronizing signal generation circuit. After passing through the sync separation circuit and burst separation circuit, the signals are input into phase comparator circuit IC4. The synchronizing signal that is input in pin (17) and the HD

signal that is input in pin (15) are compared with each other, and the result is output as H COM OUT signal through pin (9) . Similarly, the EXT SC signal that in input into pin (4) and SC COM OUT signal through pin (1) . Using these signals, VCO, X001 & VCO, X002 send the reference signals to the synchronizing signal generation circuit IC6. IC6 can output various gain locked signals with VCO1 & VCO2.

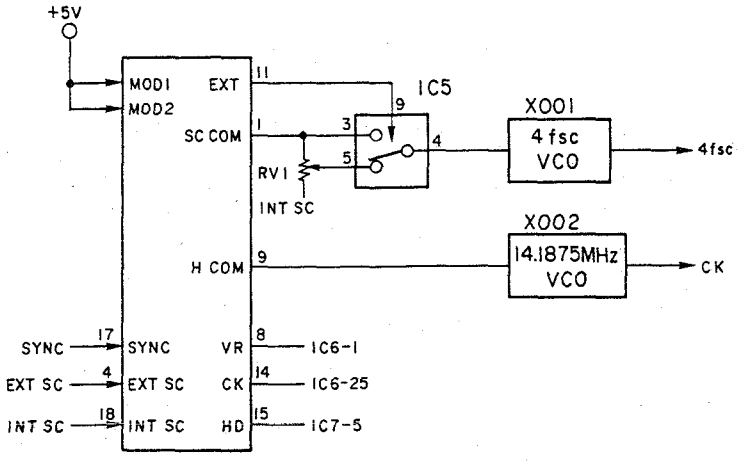


Fig. 2-10 Genlock drive and synchronizing signal generation circuits

2-10 CHROMA CLAMP CIRCUIT

The B-Y signal extending from TB-10 substrate passes through LPF in order to eliminate clock noise from it, and it is then input to the switcher IC443, via IC441 AMP. This switcher switches over between PB and EE. The B-Y signal, after passing through the switcher, is clamped by Q443, its blanking level is then adjusted by IC444, next it is output as a clamped B-Y signal, and finally it is input into the chroma encoder circuit of next stage.

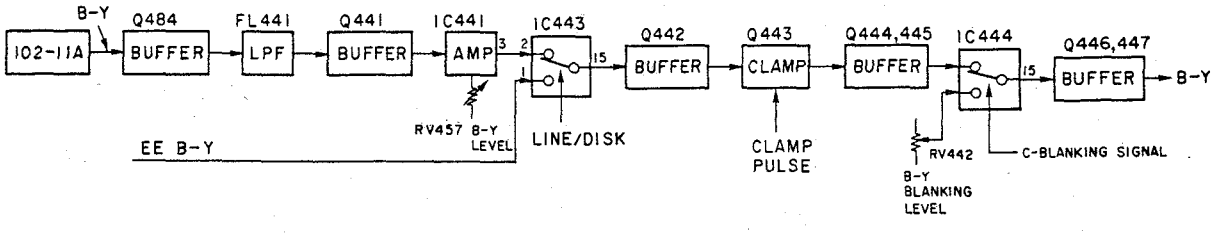


Fig. 2-11 Chroma clamp circuit

2-11 Y CLAMP AND REFERENCE SYNC ADDED CIRCUITS

The time axis corrected Y-signal that is input from TB-10 substrate is subject to elimination of clock noise of TBC by a low-pass filter, and it is then input into IC443 switcher, via IC449 AMP. This switcher switches over between PB or EE. The Y signal, after passing through the switcher, is clamped by Q465, and SYNC signal is added to it by IC451.

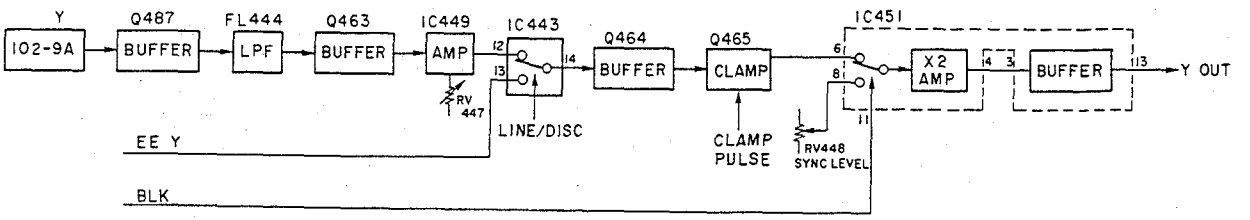


Fig. 2-12 Y clamp and reference sync added circuit

2-12 CHROMA ENCODER

The clamped B-Y signal is input into IC446, and it is ten encoded into a composite signal by subcarrier. R-Y signal also is similarly processed and encoded. The encoded signals are then mixed inside IC446 and output as composite chroma signal, via 4.43 MHz and pass-filter.

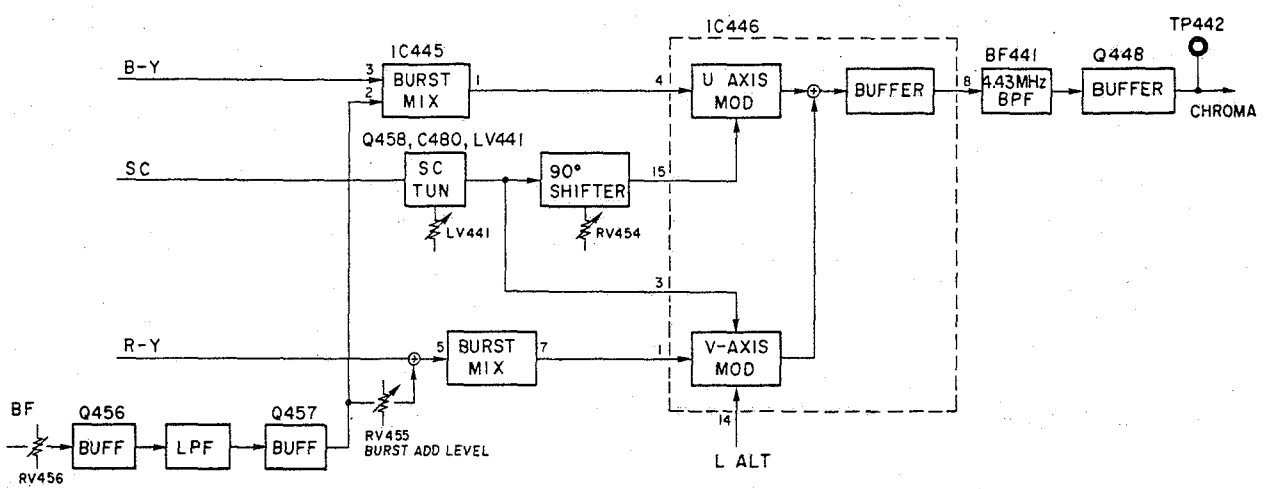


Fig. 2-13 Composite chroma encoder circuit

2-13 COMPOSITE VIDEO SIGNAL PROCESSING

The Y-signal that is output from pin (4) of IC451 is delayed by DL441, and it is then sent to the chroma signal mixing circuit that is composed of Q470, 471. This chroma signal is the composite chroma signal generated with chroma encoder. The signal that is mixed with chroma signal becomes composite video signal, and is sent to IC456 switcher. IC456 executes the switch over between composite signal and B/W signal. Similarly, IC563 switcher executes the switch over with BYPASS VIDEO (AGC VIDEO). After covering IC456, 563, the composite video signal is sent to character mix circuit, where it is output through CN102 23A.

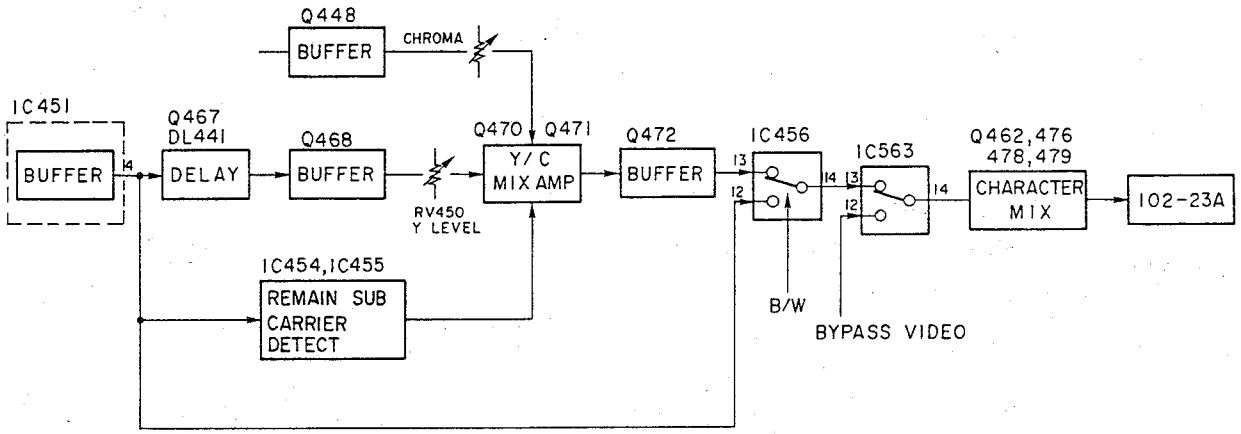


Fig. 2-14 Composite video signal processing system

2-14 COMPONENT SYSTEM CHROMA SIGNAL

The B-Y signal, after passing through clamp circuit, is sent from Q447 buffer over to RGB matrix circuit, where it is converted from B-Y into B, and is sent to IC562. IC562 selects B-Y or B. Next, it is output through CN102 21A, via IC565, 564. IC565 supplies Y-signal to B channel, while in B/W mode; and IC564 mutes the B channel, while in B/W mode or Y, R-Y, B-Y output mode. R-Y signal also is processed by identical circuit.

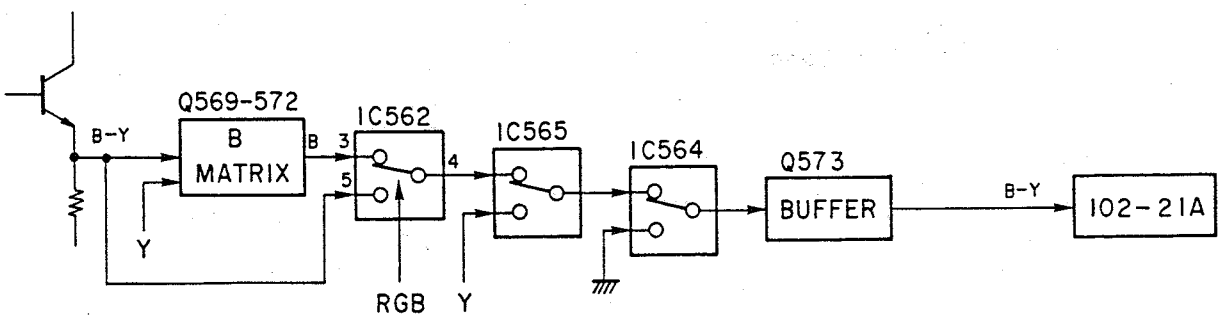


Fig. 2-15

2-15 COMPONENT SYSTEM Y-SIGNAL

The Y-signal that is output through pin (13) of IC451 is sent to character mix circuit; at the next stage, its SYNC part is muted by IC563, and then it is sent to IC563 (2/3). IC563 (2/3) selects whether or not to mute the SYNC part. After passing through IC563, the Y-signal is supplied to G matrix circuit, where it is converted from Y into G. IC562 is the switcher of select Y or G. IC565 selects Y-signal at the time of B/W mode. After passing through Q568, the signal is output to CN102-20A.

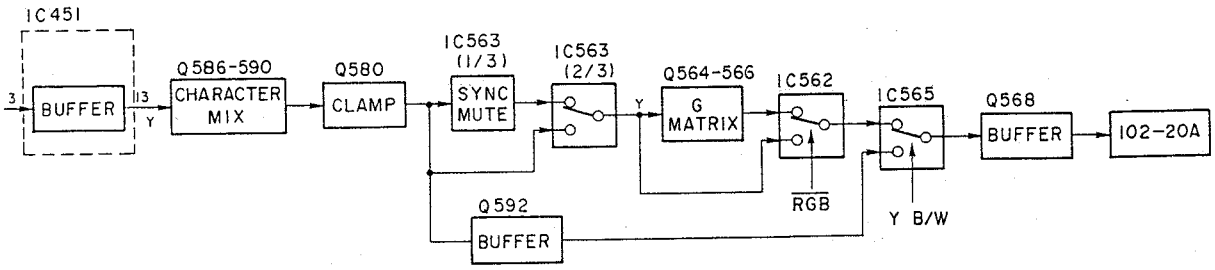


Fig. 2-16

2-16 CHARACTER MIX CIRCUIT

The video signal that in input in Q462 is SYNC TIP clamped by Q480, it then passes through Q476 buffer, and the background of its character insert part is then attenuated to 1/2 level. Next, character is mixed with it by Q479.

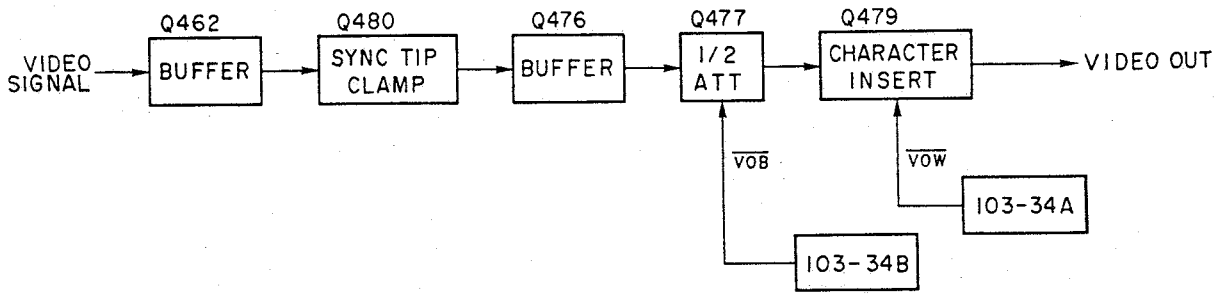


Fig. 2-17

3. TB-10 BOARD

As seen in the general block diagram of Fig. 3-1, TB-10 is composed of 4 blocks and another 1 block of a deep VM-12 board which substitutes for the TB-10 board. At first, the role of TB-10 played in the flow of general signal processing is an shown in Fig. 3-2. Each block of TB-10 is successively described next.

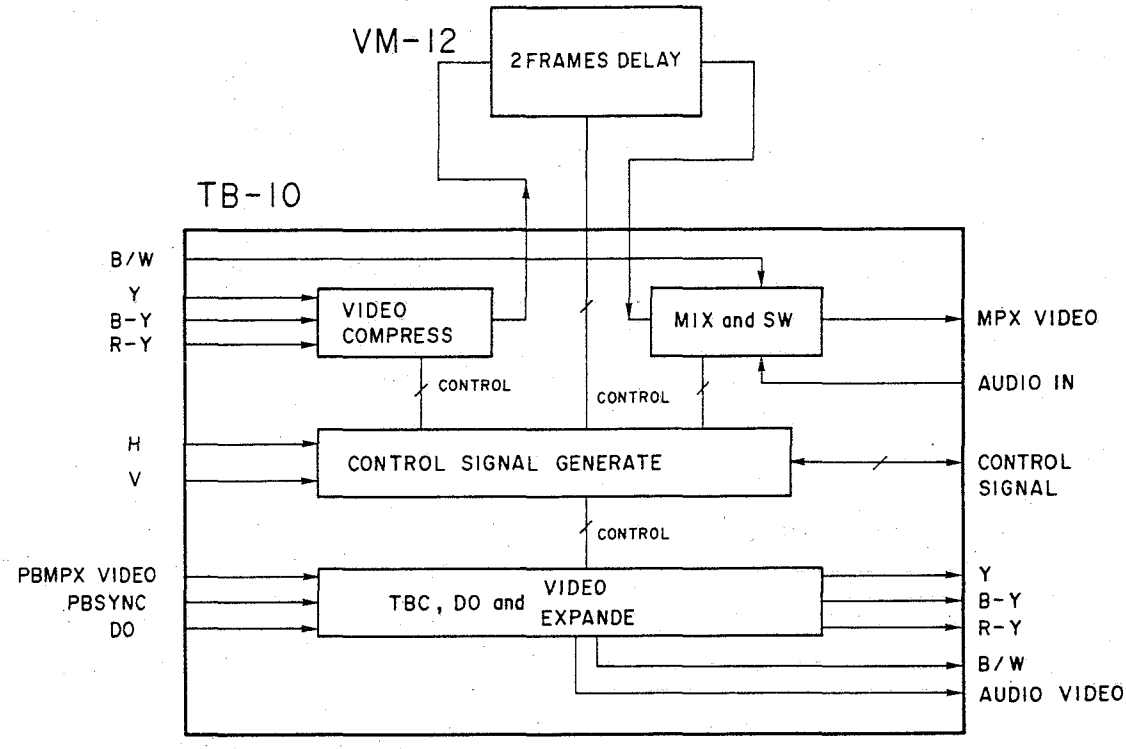


Fig. 3-1 TB-10 block diagram

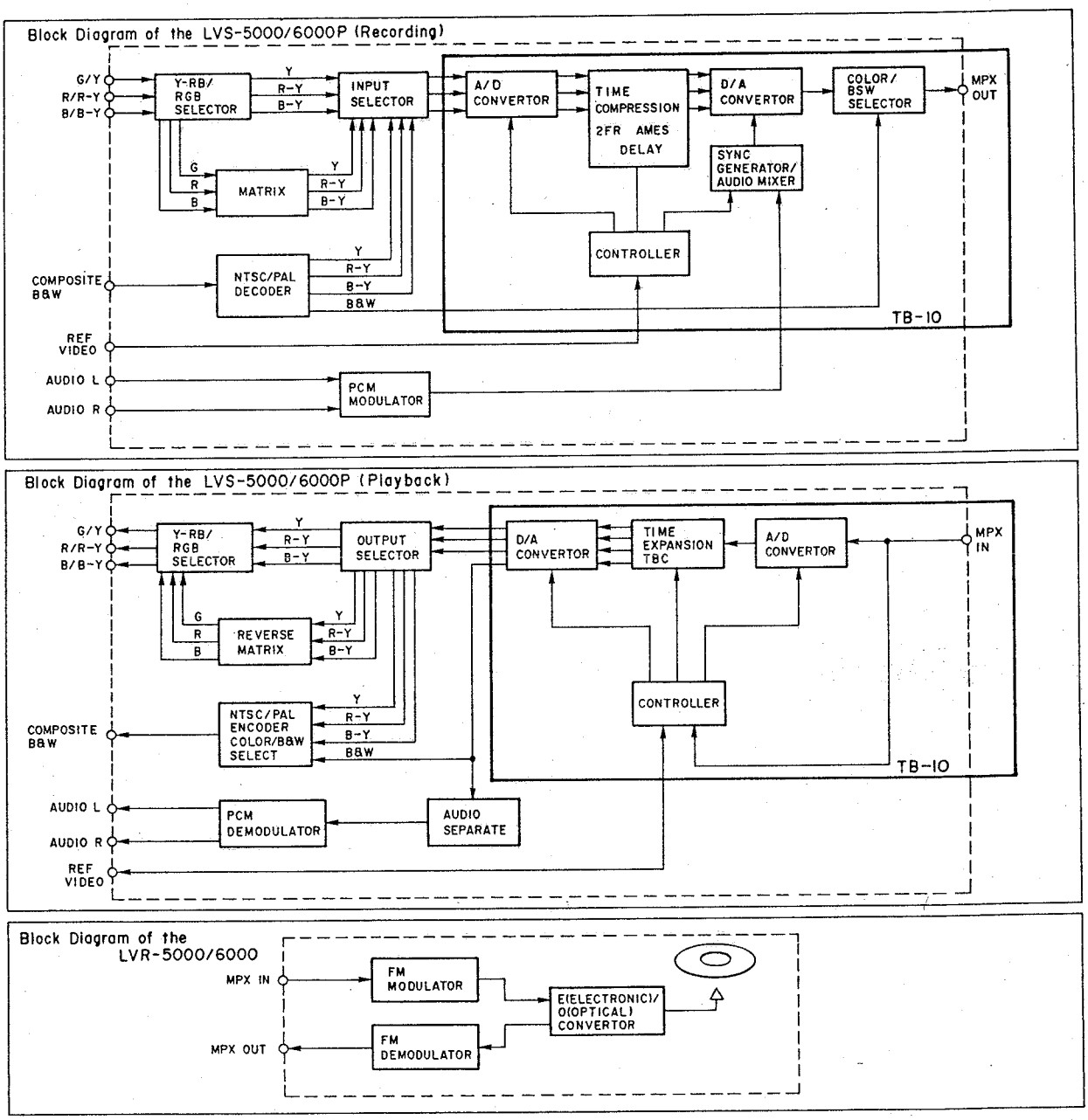


Fig. 3-2 Overall signal flow

3-1 CONTROL SIGNAL GENERATE (CONTROL SIGNAL GENERATING BLOCK)

Basic configuration of the control signal generator, which generates various gate signals with H and V timings, is as shown in Fig. 3-3.

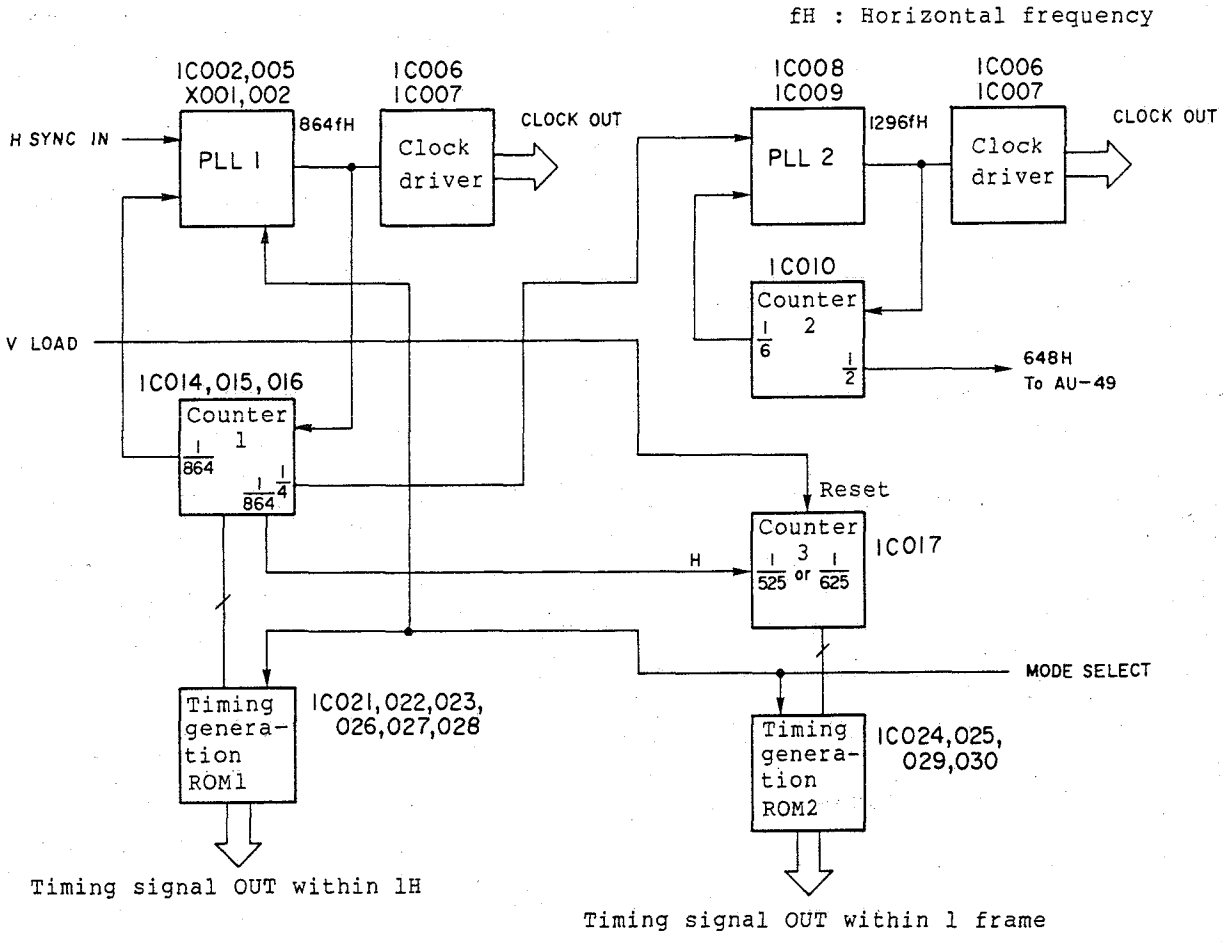


Fig. 3-3 Block diagram of control signal generator

Timing signal within 1H and timing signal within 1 frame are gate signals which repeat after every 1H cycle of 1 frame cycle, as shown in the example of Fig. 3-4.

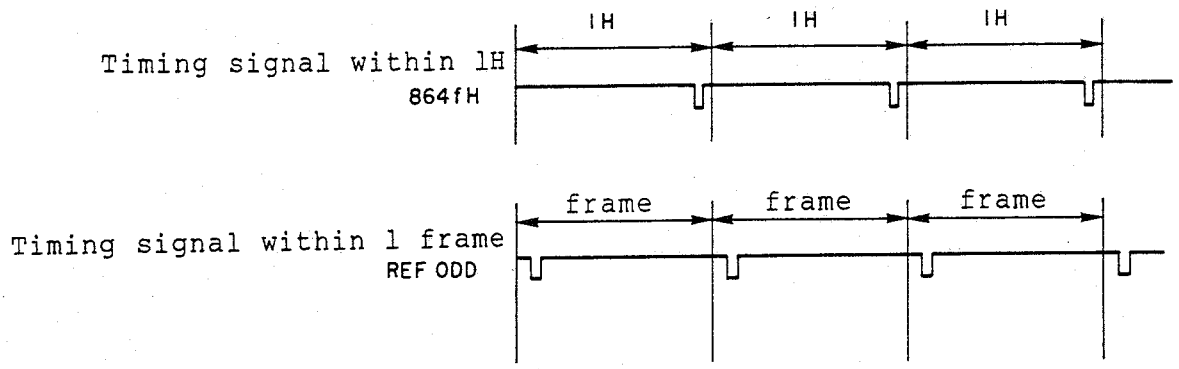


Fig. 3-4 Example of timing signal within 1H and timing signal within 1 frame

At first, PLL1, counter 1, and timing generation ROM1 are described. Receiving H SYNC,which becomes the reference, clock 864 times larger than it is prepared. This clock serves as the sampling pulse at the time of A-D conversion of video signal; and it is further divided for serving as timing signal within 1 H. Similarly, it becomes the read clock of TBC at the time of reproduction. Next, counter 3 and timing generation ROM2 receive the frequency of H, with the output of counter 1, and prepare the timing signal within 1 frame by counting it up. This counter 3 is reset by VLOAD signal, whereby frame synchronization is done.

PLL2 and counter 2 prepare a clock 1296 times larger than H, in synchronization with the output of PLL1. This clock becomes the read clock of FIFO at the time of compressing video signal. The clock that has been counted down to 1/2 becomes the reference clock of audio data signal. These 864 fH and 1296 fH clocks are distributed by clock drivers IC006, IC007; but at the time of recording by the system the clocks of reproducing side are stopped; while at the time of reproduction, the clocks of recording side are stopped. And, the 648 fH clock is sent to audio board AV-49 by IC011.

3-2 VIDEO COMPRESS (VIDEO TIME AXIS COMPRESSION BLOCK)

This block is composed of A-D conversion and the FIFO for time axis compression. Since the processing of Y, B-Y, and R-Y is identical upto the point of A-D conversion, only Y is described here. The input Y-signal is restricted to 5 MHz band by FL001 (LPF). Next, its gain and DC level are adjusted by IC041, so as to make it enter the dynamic range of A-D converter IC066 (CXA1096M). After A-D conversion, the data of Y enters FIFO IC189, and is compressed 1.5

times. B-Y and R-Y signals also are compressed similarly by 6 times. This condition is as shown in Fig. 3-5.

In this way, the time division multiplexed component signal is sent to VM-12 board for being synchronized, and is delayed by 2 frames.

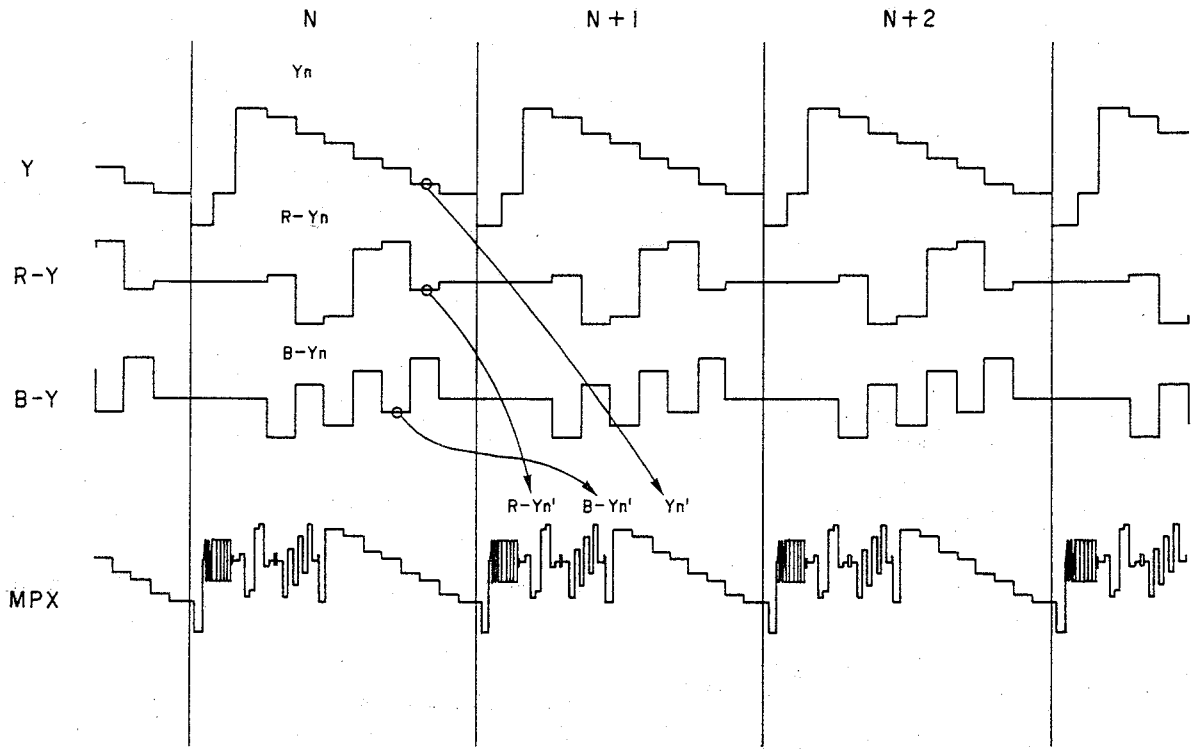


Fig. 3-5 Time compression

3-3 VM-12 BOARD (2 FRAME DELAY BLOCK)

VM-12 board, which is a smaller version of TB-10 board, plays the role of delaying the time division multiplexed Y, B-Y, R-Y signals by only 2 frames, for the purpose of synchronizing them with audio signal. Toward that goal, the 1M bit video RAM, which is composed of the twelve IC003 to IC014, operates as a shift register.

3-4 MIX AND SW

This block is composed of the Y, B-Y, R-Y signals which are delayed by 2 frames after passing through VM-12 board, digital audio signal sent from AU-49 board, the circuit which executes time division multiplexing of burst SYNC, and a circuit to switch over between the prepared MPX signal and B/W signal. It is as shown in Fig.3-6.

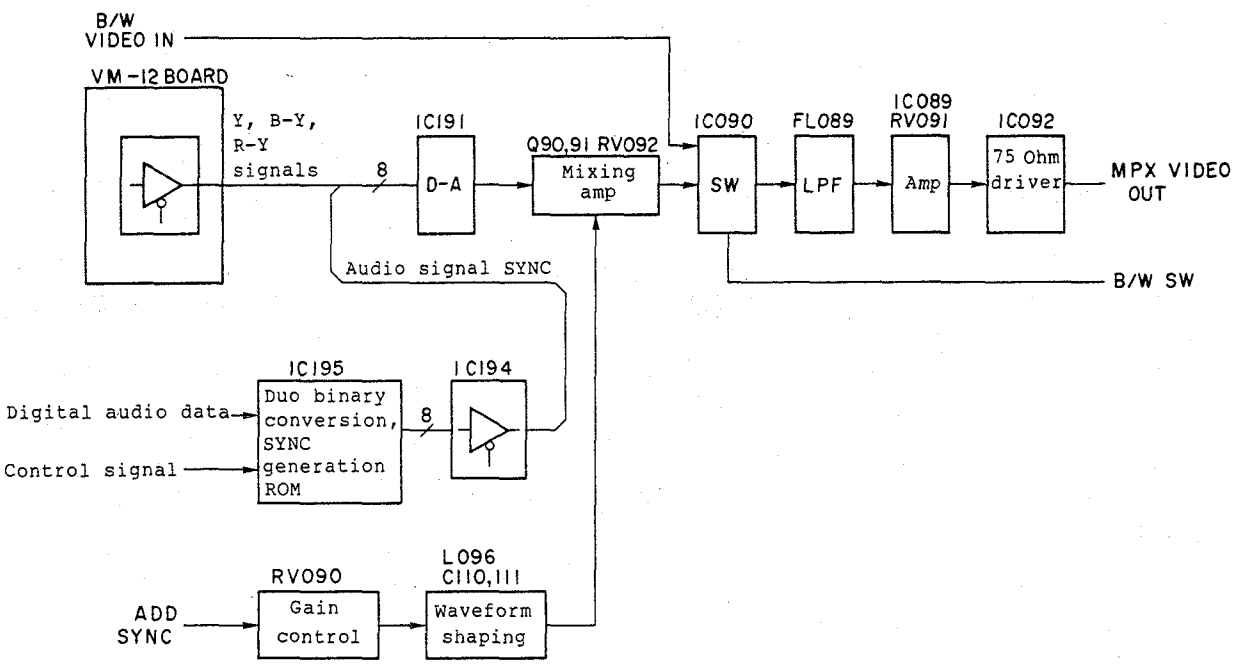


Fig. 3-6 Block diagram of audio MIX, color, and B/W

3-5 TBC, DO AND VIDEO EXPAND

This block is composed of TBC, drop out compensation, and time axis elongation unit. To execute these 3, the input PBMPX VIDEO signal is at first A-D converted. The resultant digital signal is then subject to TBC, drop out compensation, the time axis elongation. Its block diagram is as shown in Fig. 3-8. At first, the input PBMPX VIDEO signal is delayed by 350 nsec, by DL134, in order to adjust its timing with drop out con; and after that it is A-D converted by IC135. The clock for A-D conversion contains jitter that is synchronized with PBMPX VIDEO signal≤ and the work of generating this clock is done by almost the entire TBC block. The A-D converted signal is written into the FIFO of IC212, 215, 218, 221, with the same clock; and the operations of TBC and time axis elongation are done by reading it out with the clock prepared from reference H. Next is described the generation of clock for A-D conversion. Because of the time axis manipulation, this format determines how fine precision is acquired in the detection f SYNC, at the time of reproduction. As shown in Fig. 3-7, the sign "o" indicated in PBMPX VIDEO becomes the reference for time axis, and it is detected by the SYNCGATE signal coming from PBH SYNC. The PBH obtained in this way enter PLL for the purpose of clock generation. This PLL is of the same reset type as in the well acquainted BVW-40, etc; and it is composed of the phase comparator of IC175, the VCO of Q151, D154, 155, and the 1/1296 divider of IC164, 165, 166.

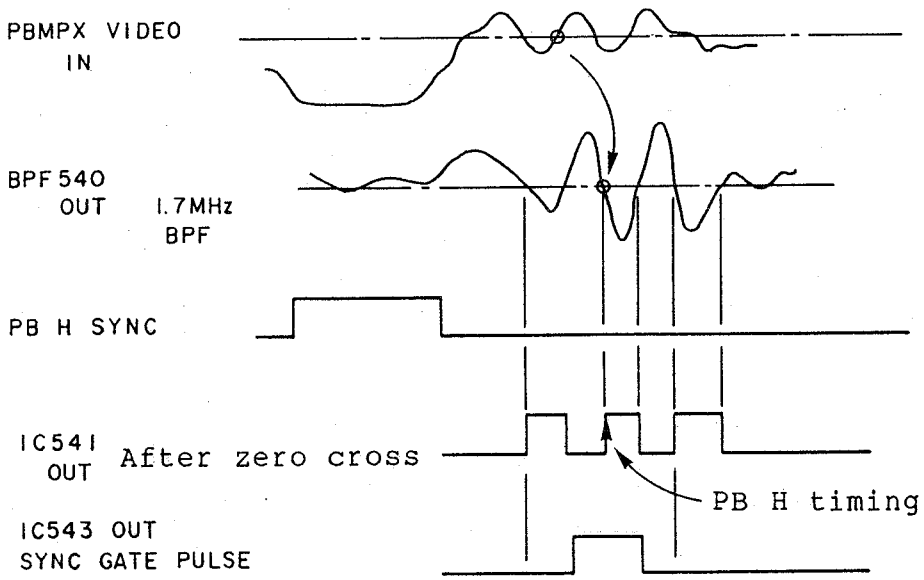


Fig. 3-7 Burst SYNC detection timing

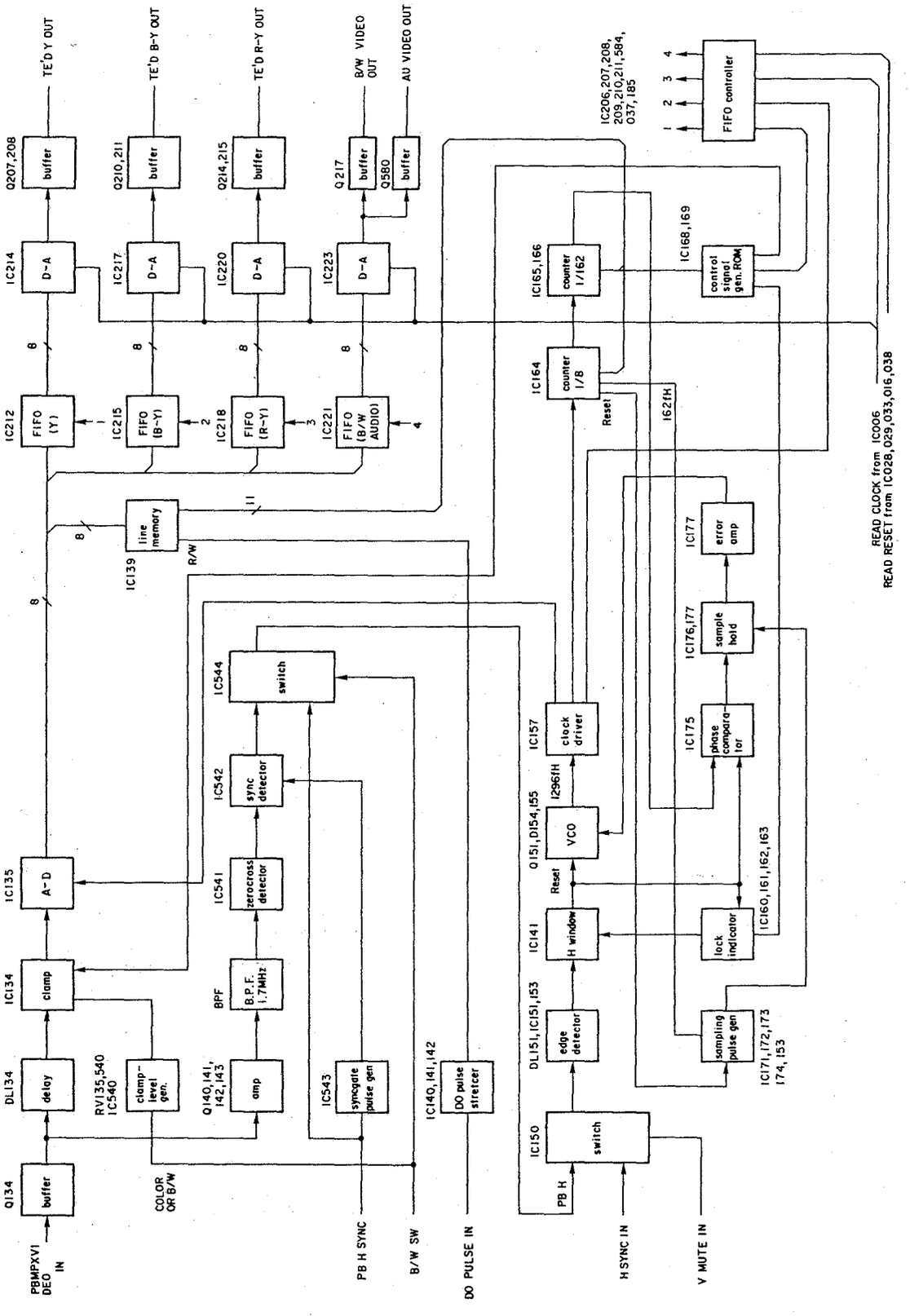


Fig. 3-8 TBC, DO and video expand block diagram

The H WINDOW of IC141 is meant for eliminating the false PBH, and its window width is about +0.5 μsec. It is equipped with lock indicator IC160, 161, 162, 163 for stopping its operation when the PBH is unsteady due to the rise of spindle. Window operation resumes as soon as the spindle becomes steady enough to permit PBH to enter the H WINDOW continuously (allowing once or twice missing PBH) 10 times. The signal to control FIFO at the time of reproduction is generated from ROM of IC168, 169, by suing the clocks obtained in this way.

The switch of IC150 is meant to prevent the PLL from becoming unstable, because of not receiving PB H SYNC at the time of reproducing unrecorded portion of the disk; and by making this arrangement, the image can be instantly picked up upon moving from unrecorded portion to recorded portion.

Line memory IC139 is provided for drop out compensation, and it is designed to keep on fetching 1H earlier data, whenever drop out occurs.

Fig 3-9 shows the elongation of time axis. The spindle is locked at the phase which is advance by about 1.4H, thereby acquiring jitter margin of about ±20 μsec.

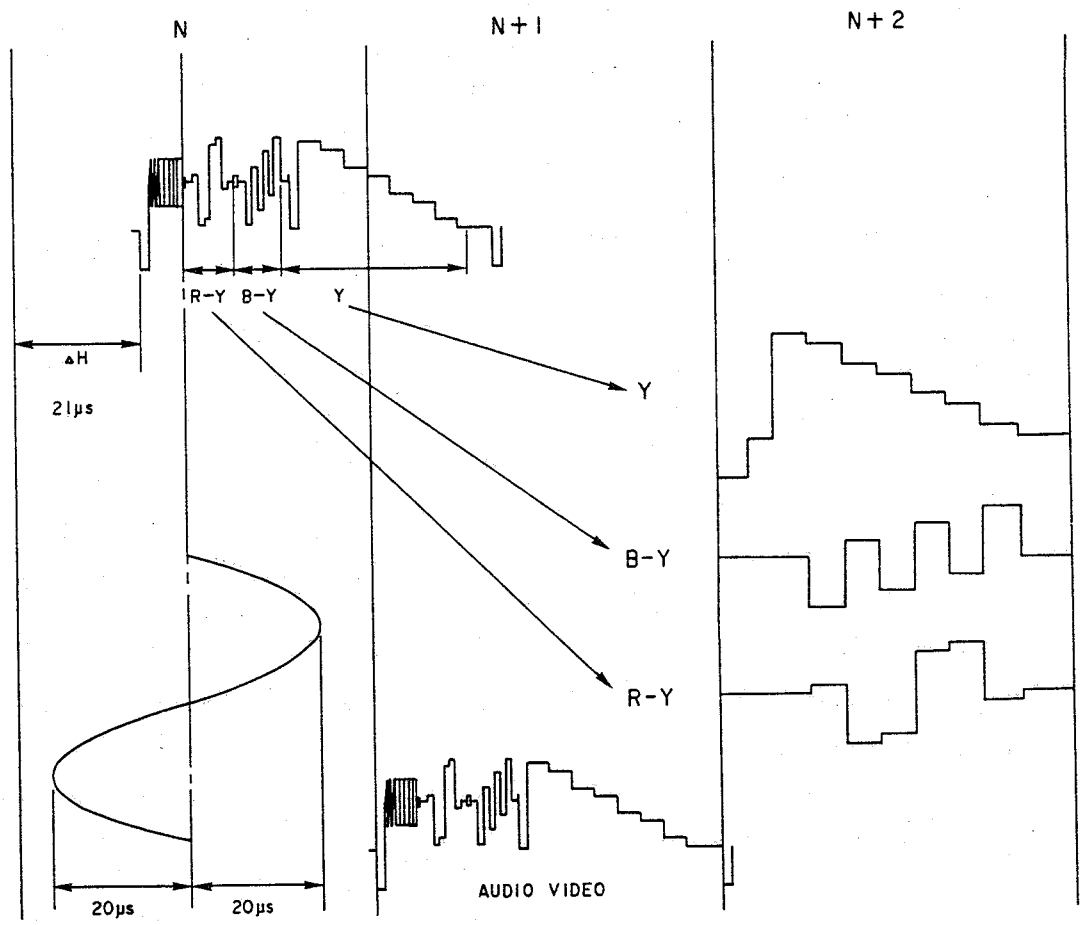


Fig. 3-9 Time expansion and time base correction

4. AU-49 BOARD (AUDIO SYSTEM)

Since the CRV disc's audio format diverts the 8mm VTR PCM format, the configuration from the analog block until PCM modulation is basically the same as that of an 8mm VTR. Most of the audio circuits are configured on the AU-49 board. They are divided into three major blocks: the analog block and the two digital blocks for the 8mm VTR format and the CRV disc format.

4-1 ANALOG BLOCK

The analog block basically consists of the following five circuits:

1. Input circuit
2. Output circuit
3. Recording circuit
4. Playback circuit
5. Peak indicator circuit

Since CH-1/L and CH-2/R have the same circuit configuration, only the CH-1/L system is described below.

4-1-1 INPUT CIRCUIT

The audio signal that is input to the connector panel's AUDIO IN CH-1/L connector (XLR type) determines whether to terminate 600 Ω with the AI-5 board. The standard level of the input signal is +4 dBs. The audio signal is then sent to the AU-49 board via the MB-16 board.

The signal that is input at a balanced level is made unbalanced by IC092. The high-pass filter in IC007 eliminates unnecessary components 20 Hz and below. This high-pass filter is a secondary active filter. It also has a -2 dB ATT for matching the level. The signal from pin (1) of IC007 is sent from CN001 to the LA-7 board. This level volume allows the recording level to the adjusted freely. When the recording level is adjusted to 0VU, its output level becomes +4 dBm.

The signal that passes through the level volume is input to pin (2) of IC015. This IC is also an equalizer which slightly raises the low-band frequency characteristics for the 10 dB gain amplifier. The signal that is output from pin (1) of IC015 is lowered by 4 dB by R150 and R151 to match the level. The signal then branches off to the EE system, which sends the signal to the output circuit, and to the REC system which inputs the signal to pin (11) of IC014.

4-1-2 OUTPUT CIRCUIT

The EE system signal that is output from pin (1) of IC015 passes through the resistor ATT, then it is input to pin (13) of IC006. Meanwhile, the playback signal from the disc is output from pin (9) of IC011 and input to pin (12) of IC006. IC006 is a EE/PB signal changeover switch. The signal that is changed over here is output from pin (14) and input to IC005.

IC005 changes over and mutes CH-1/L and CH-2/R. For example, if CH-1/L is muted, the sound for CH-2/R is output from both channels. And if CH-2/L is muted, the sound for CH-1/L is output from both channels. The signal that is output form pin (13) of IC005 passes through Q015, then it is input to pin (3) of IC003. Q015 is transistor that prevents click noise.

IC003 is the first step's output amplifier, and it has a 17dB gain. The signal that is output from pin (1) of IC003 branches off into three signals that are respectively sent to pin (7) of IC091 at the final step, pin (5) of the level meter drive circuit IC004, and to the HP-46 board (via the MB-16 board) that has the headphone volume.

The signal that is input to pin (7) of IC091 at the final step is converted from an unbalanced level to a balanced level. Then it is output from pins (10) and (9) . After passing through the MB-16 board, the signal is output from the connector (XLR type) on the rear panel. The standard level is +4 dBm.

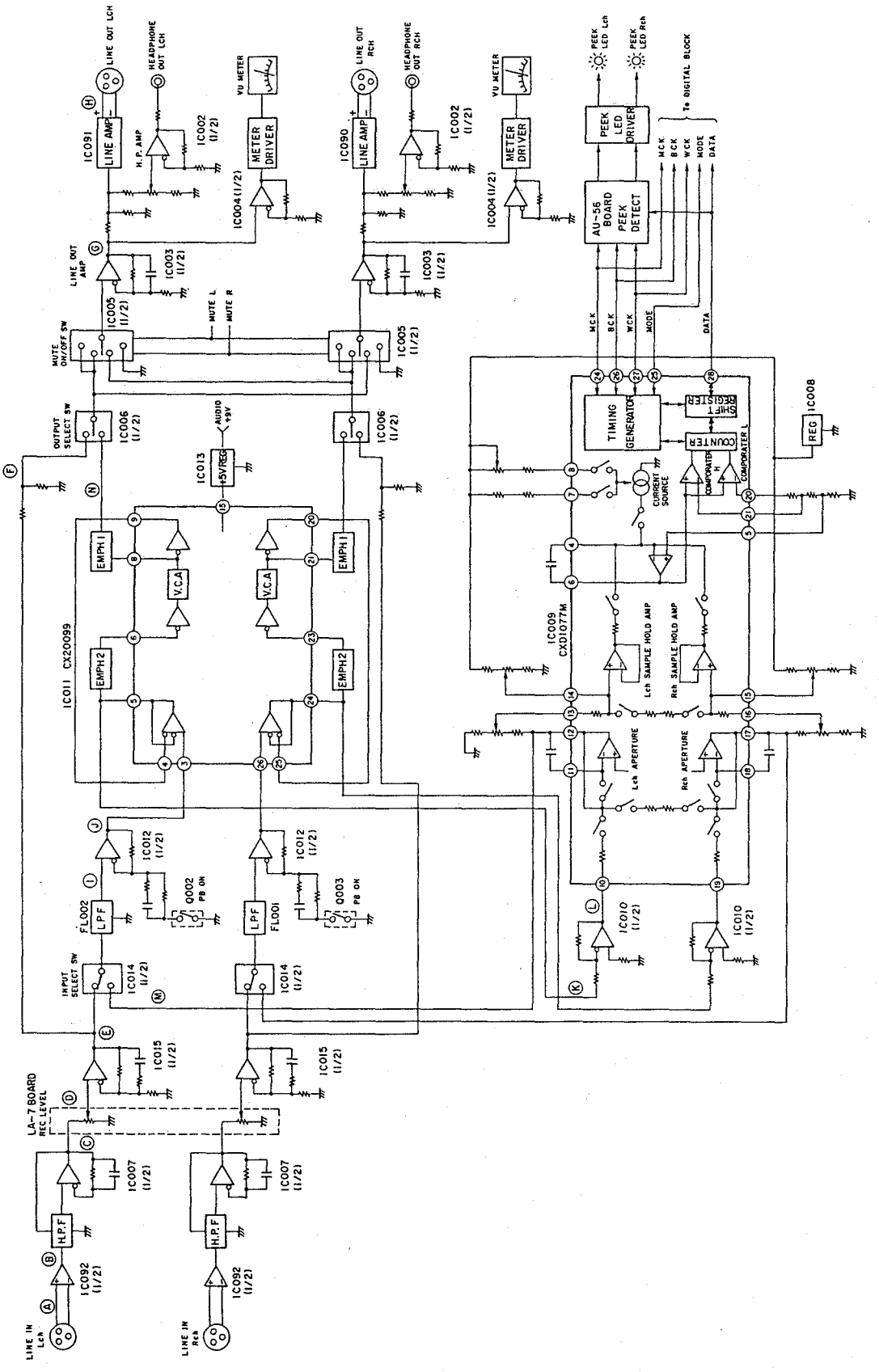


Fig. 4-1 Analog audio block diagram

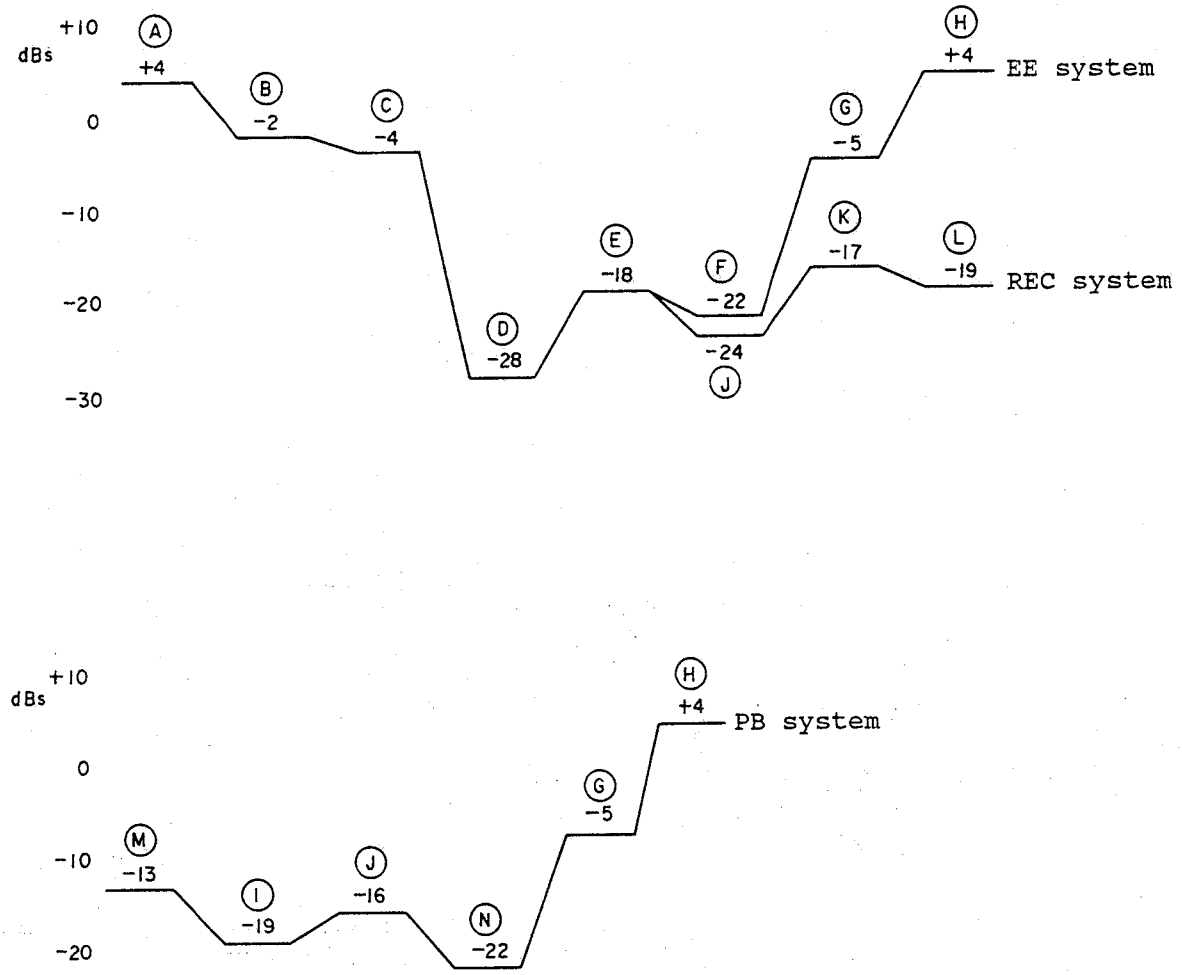


Fig. 4-2 Level diagram

4-1-3 RECORDING CIRCUIT

This circuit also serves as the playback circuit. The SW allows the circuit to changeover between the REC/PB functions. The signal from pin (1) of IC015 is input to pin (11) of the REC/PB changeover switch IC014. The signal is then output from pin (13) . Next, the FL002 low-pass filter eliminates the unnecessary components at 15 kHz and above. After passing through IC012's buffer, the signal is input to IC011 noise reduction. IC012's function differs for REC and for PB. For REC, it serves as a buffer. For PB, it serves as an aperture compensation equalizer. Q002 changes over the IC012's functions.

(1) 15 kHz low-pass filter

This low-pass filter is one part that determines the CRV disc's audio portion's frequency characteristics.

PCM is a digital signal that was converted from an analog signal which was cut away to the time base direction (sampling) and to the level direction (quantization). When sampling is to be done, it must be done at a frequency at least twice that of the signal's maximum frequency, according to the sampling theorem. Since the CRV disc's PCM audio system diverts the 8mm VTR's PCM format, the sampling frequency is 31.5 kHz (2fH). Therefore, the maximum frequency the PCM audio system can handle is 15.75 kHz. Thus, before the audio signal undergoes sampling, the low-pass filter eliminates the high frequency components 15.75 kHz or above.

(2) Noise reduction circuit

In order to compensate for the digital section's dynamic range deficiency, the CRV disc's PCM audio system employes an analog noise reduction system.The signal that was input from pin (3) of IC011 is input to MOA (main operation amplifier). During REC, MOA is an operation amplifier which sets pin (3) as positive input and pin (4) as negative input. For MOA's negative input pin (4) , in order to return the signal that was lowered from a high-band level by the emphasis 2 and emphasis 1 circuits (both fixed emphasis circuits) configuring CR, MOA's gain is increased at the high band and pre-emphasis is performed. Also, the more the VCA (voltage control amplifier) decreases the gain, the lower the DET (detection) circuit's input level becomes. Thus, the more the level of the signal being input to the DET circuit input (pin (11)) decreases, the more MOA's negative feedback amount decreases, and MOA's gain increases. The signal is then compressed (2:1). When this happens, the DET circuit input is added with the wairing circuit which has frequency characteristics reverse that of the emphasis 2 circuit. If only a high-band component signal is input, the VCA's gain is increased, and the emphasis amount of the emphasis 2 circuit is

negated. Also, the NR circuit's attack time, recovery time, and hold time are determined by capacitor pins (12) and (13).

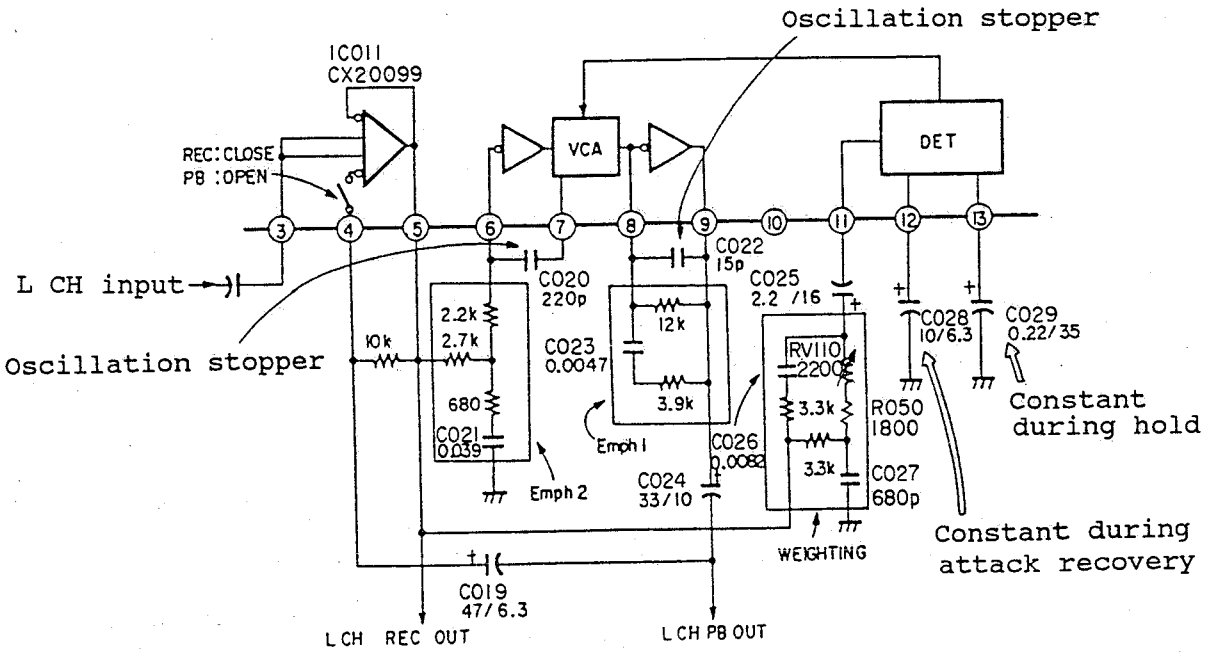


Fig. 4-3 NR circuit

(3) A/D conversion circuit

IC009 (CXD1077M) is a cascade integrated type, 10-bit A/D-D/A converter. The signal that is output from pin (5) of IC011 is input to pin (2) of IC010. The reverse amplifier reduces the gain by 2 dB, and the signal is output from pin (1). Then it enters the A/D converter (IC009) for conversion into 10-bit DATA.

The analog input signal added to pin (10) of IC009 is amplified by about 6 dB by the aperture amplifier. Then it is output to pin (12) of the aperture output terminal. After this output signal

undergoes the elimination of components outside the band by the external anti aliasing filter, it is added to pin (13) of the S/H amplifier input terminal. Then the signal is amplified by about 9.25 dB by the S/H amplifier and output to pin (6) of the integrated output terminal. Next, by inputting WCK from pin (27) and BCK from pin (26) , the C. C. (convert command) is generated internally. When C. C. is in interval "H", the analog signal that was added to the S/H amplifier undergoes sampling. When C. C. is in interval "L", the integrated circuit integrates the input signal and the constant current which has been weighted with reversed polarity. This allows the conversion operation. By using the respective counters to calculate the integration of the rough constant current and the integration time of the detailed constant current, the 10-bit data is ascertained. When C. C. is in "H" again, this data is loaded to the shift resistor and output in serial, synchronized with the startup of BCK and LSB as the leader. The data code is 2's complement.

The 10-bit data output from pin (28) of IC009 is sent to the digital processing circuit (IC024) and the peak indicator circuit (IC095). Note that pin (28) serves as a data output terminal during REC, and as a data input terminal during PB.

[Offset adjustment]

Like the 8mm VTR's PCM system, the CRV disc's PCM audio system uses non-linear quantization by the 10-bit ↔ 8-bit compression/expansion of the digital data. Consequently, if the direct current offset is included in the A/D converter's data output, the distortion will increase. In order to compensate for this direct current offset, an offset voltage is added from the offset compensation terminal (pin (14) of IC009). In a no signal input condition, adjustment is made so that the data output becomes "00000000".

[Operation principle of the A/D converter]

The electrical charge for the analog voltage that was input is accumulated by the integrator's capacitor. Integration is done through the constant current of the reverse characteristics. The time counted by the digital counter is made into data.

[Operation principle of the D/A converter]

Having the reverse operation of the A/D converter, the D/A converter has clock counting of only the input's digital data amount. During the counting period, the output voltage that corresponds to the digital data is obtained through the integration of the constant current.

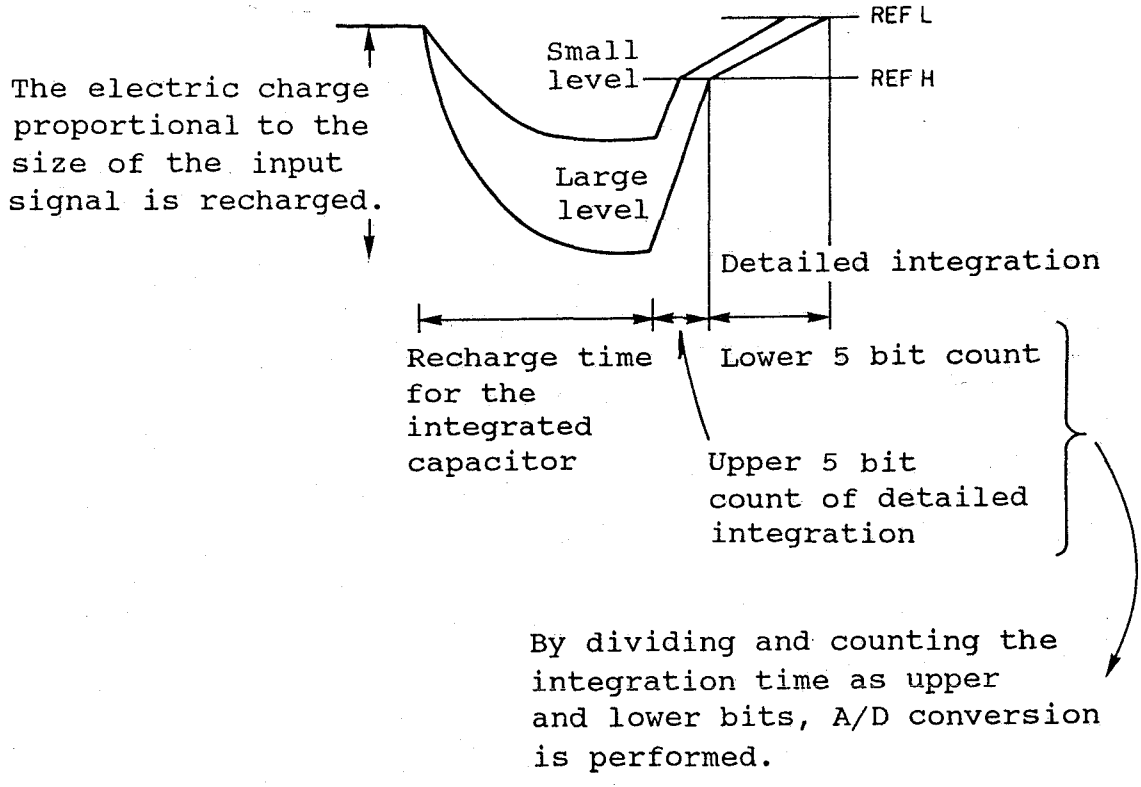

REF L
Small level
REF H
The electric charge proportional to the size of the input signal is recharged.
Large level
Detailed integration
Recharge time for the integrated capacitor
Lower 5 bit count
Upper 5 bit count of detailed integration
By dividing and counting the integration time as upper and lower bits, A/D conversion is performed.

Fig. 4-4 Operation pinciple of the A/D and D/A converters

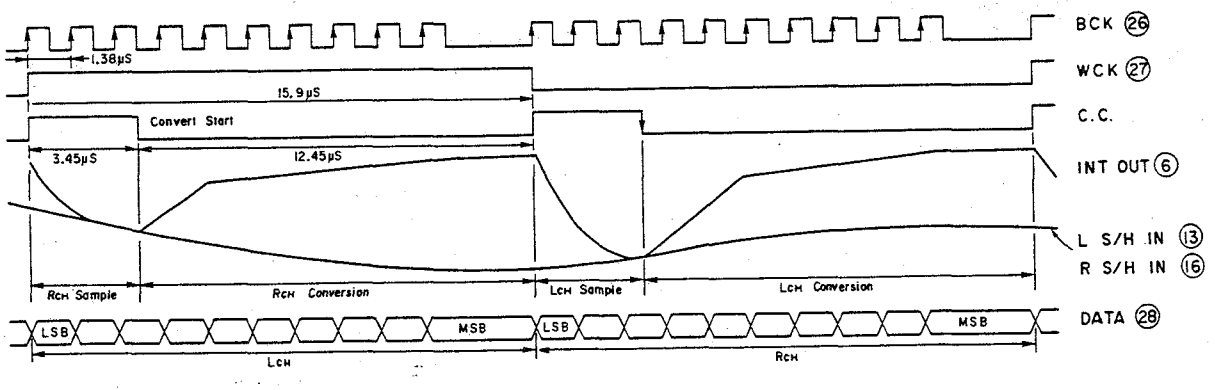


Fig. 4-5 Timing chart in the REC mode

4-1-4 PLAYBACK CIRCUIT

The playback circuit also serves as the recording circuit. The circuit is used for playback after being switched over for playback by a switch.

(1) D/A conversion circuit

The 10-bit serial data sent by the digital processing section is input to pin (28) of IC009. When wck is input from pin (27) and BCK is input from pin (26) , DIS (discharge clock) and APT (aperture clock) are generated internally. Also, the serial data, which input LSB as the leader, is taken in by the shift resistor after synchronization with the startup of BCK. In interval "H", DIS is set to the counter. When DIS is in "L", the counter starts counting from the value that was set. The weighted constant current that corresponds to the data is also output. When the counter outputs the carrier signal, the counting and the constant current output are terminated.

The analog block first discharges the integrated charge of the previous conversion. This is done by using the integrator for sampling the external standard voltage of 3.6 V which was added to pin (20) , with DIS in interval "H". As a result, the integrated output is initialized to about 1.8 V in the discharge interval. The output midpoint becomes about 2.5 V when the sine wave data is input. When DIS is in "L", D/A conversion is performed by integrating the constant current output. When the constant current output stops, the integration will also stop. However, the terminal voltage that is held for the integration capacity becomes the D/A conversion value.

This terminal voltage is amplified by about 1.6 dB by the aperture amplifier and output to pin (12) of the aperture output terminal. The waveform during this time becomes an on-step waveform.

Pin (8) of IC009 is a terminal which discharges the integrated current during D/A conversion. However, since the integrator's output voltage is determined by the integrated current value, the variable resistor (RV105) adjusts the D/A gain to adjust the PB level.

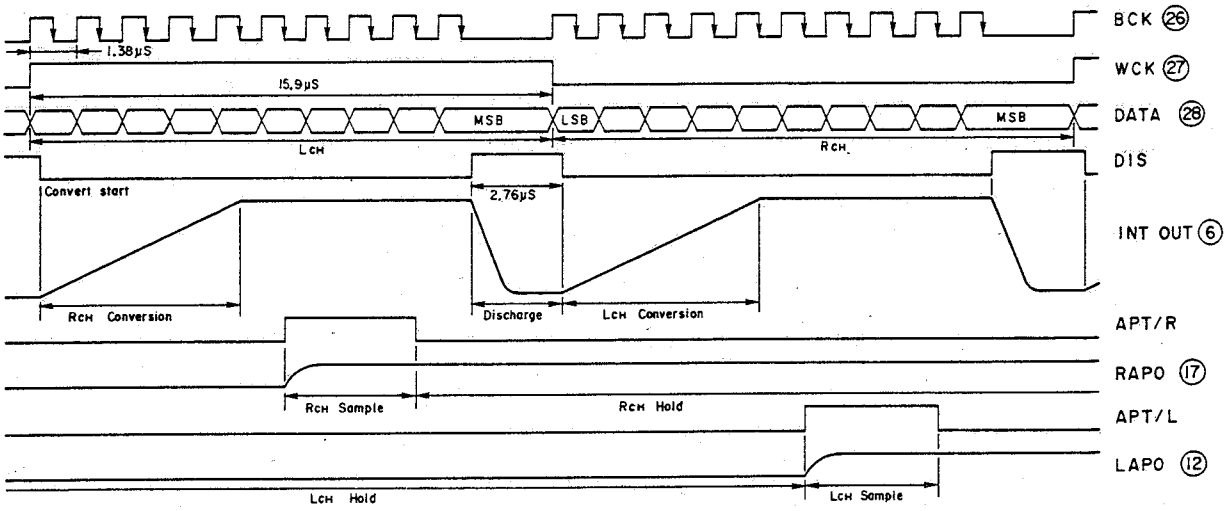


Fig. 4-6 Timing chart in the PB mode

(2) Low-pass filter and aperture compensation circuit

The signal that has undergone D/A conversion is output from pin ⑫ of IC009, then it enters pin ⑮ of IC014, which is the REC/PB changeover switch. And after the signal is output from pin ⑬ , it is input to FL002. The signal that has undergone D/A conversion has unnecessary spectrum that was produced during the sampling. Therefore a 15 kHz low-pass filter is used to eliminate this spectrum. Since the cutoff frequency is the same as during REC, the filter for REC is used.

After passing through FL002, the signal is input to pin ⑤ of IC012. This circuit is only a buffer amplifier during REC. However during PB, it serves as an equalizer amplifier for aperture compensation.

Aperture compensation works as follows: In the case where the signal has undergone sampling, ideally the sampling's pulse width must narrow infinitely, otherwise the signal cannot be demodulated completely. If this pulse width becomes wide, the frequency characteristics after demodulation will be degraded in the high band. The CRV disc uses an equalizer having reverse characteristics to compensate for these degraded frequency characteristics. Note that this equalizer is also a 3 dB amplifier.

(3) Noise reduction circuit

The audio signal that has been compressed and preemphasized during REC is returned to its original state after expansion and de-emphasis. As a result, the level of the noise generated during the recording and playback processes decreases relatively to achieve noise reduction. The signal that is input from pin (3) of IC011 is input to MOA. MOA operates as a buffer amplifier during PB. The emphasis 2 and emphasis 1 circuits lower the high band level of the buffer amplifier output's audio signal, which is also de-emphasized. Also, the more the gain of VCA decreases, the more the DET circuit's input level decreases. The signal is expanded (1:2). During this time, the DET circuit input is added with the emphasis 2 circuit and the waiting circuit which has reverse frequency characteristics. When only the high band signal component is input, VCA's gain increases and the emphasis amount is negated by the emphasis 2 circuit.

As explained above, the audio signal that has returned to its original state after undergoing re-emphasis and expansion is output from pin (9) of IC009 and input to pin (12) of IC006, which is the EE/PB changeover switch.

4-1-5 PEAK INDICATOR CIRCUIT

The peak indicator operates only for input signals that aims to record. Thus, it does not operate for playback signals from a disc.

The 10-bit digital data that is output from pin (28) of IC009 is input to pin (1) of shift resistor IC094 after passing through IC095. The data undergoes serial-parallel conversion, and the upper 7-bits are sent to IC096, a comparator. When all the upper 7-bits of data are "H", a $\overline{\text{FULL BIT}}$ signal is output from pin (19) of IC096. After a channel (either CH-1/L or CH-2/R) is recognized, the signal is sent from CN004 to the AU-56 board.

The $\overline{\text{PEEK L}}$ signal that was sent to the AU-56 board is input to pin (1) of IC104. This IC is a down counter and can vary the count by SW002. Normally, the lower 2-bits are set to "H". Therefore if $\overline{\text{PEEK L}}$ is input four consecutive times, the $\overline{\text{PEEK L DELAY}}$ signal is output from pin (14) of IC104 and returned to the AU-49 board from CN004.

The $\overline{\text{PEEK L DELAY}}$ signal that was returned to the AU-49 board enters pin (5) of IC099. Then it is converted into a pulse having a length of about 16 ms and output from pin (7) as PEEK LED L. This signal is sent from CN002 to the VU-1 board, and D001 lights.

4-2 DIGITAL BLOCK

4-2-1 OUTLINE

In the digital audio system, an error correction code is added to the 10-bit digital audio data (ch 2) which was sampled at about 31.5 kHz. The data is then converted into the analog WO format and recording or playback is performed.

For recording, the 10-bit data which passes through the A/D converter is compressed into 8-bits and added with an error correction code. The data is then converted into the analog WO format and added with audio SYNC. And the data is delivered in digital to he TB-10 board.

For playback, the multiplex video signal played back from the disc passes through TBC, then it is input to the AU board. The audio data multiplexed through time sharing into the multiplex video signal that is input is made binary. After error correction, the 8-bit data is expanded to 10-bits and input to the D/A converter.

During recording and playback, the 8mm VTR digital audio processing ICs (CX23011 and CX23012) are used for encoding and decoding the error correction code.

4-2-2 BLOCK DIAGRAM

A block diagram of the digital audio system is shown on the next page.

The circuit comprises the 8mm PCM audio signal processing ICs (IC24 and IC23), a clock generator (IC25) synchronized with these ICs, the audio memory section (AU-57 board) which converts the 8mm PCM audio format into the analog WO audio format and vice versa, the audio memory section's control circuit, the duo-binary modulation circuit (IC37, 66) which layers the signal on the video signal during recording, and the audio SYNC detection circuit and the duo-binary demodulation circuit (IC18, 66) for playback. Also, there is the bi-phase modulation circuit (IC59, 73) and the demodulation circuit (IC55, 56) for interfacing the 8mm PCM IC.

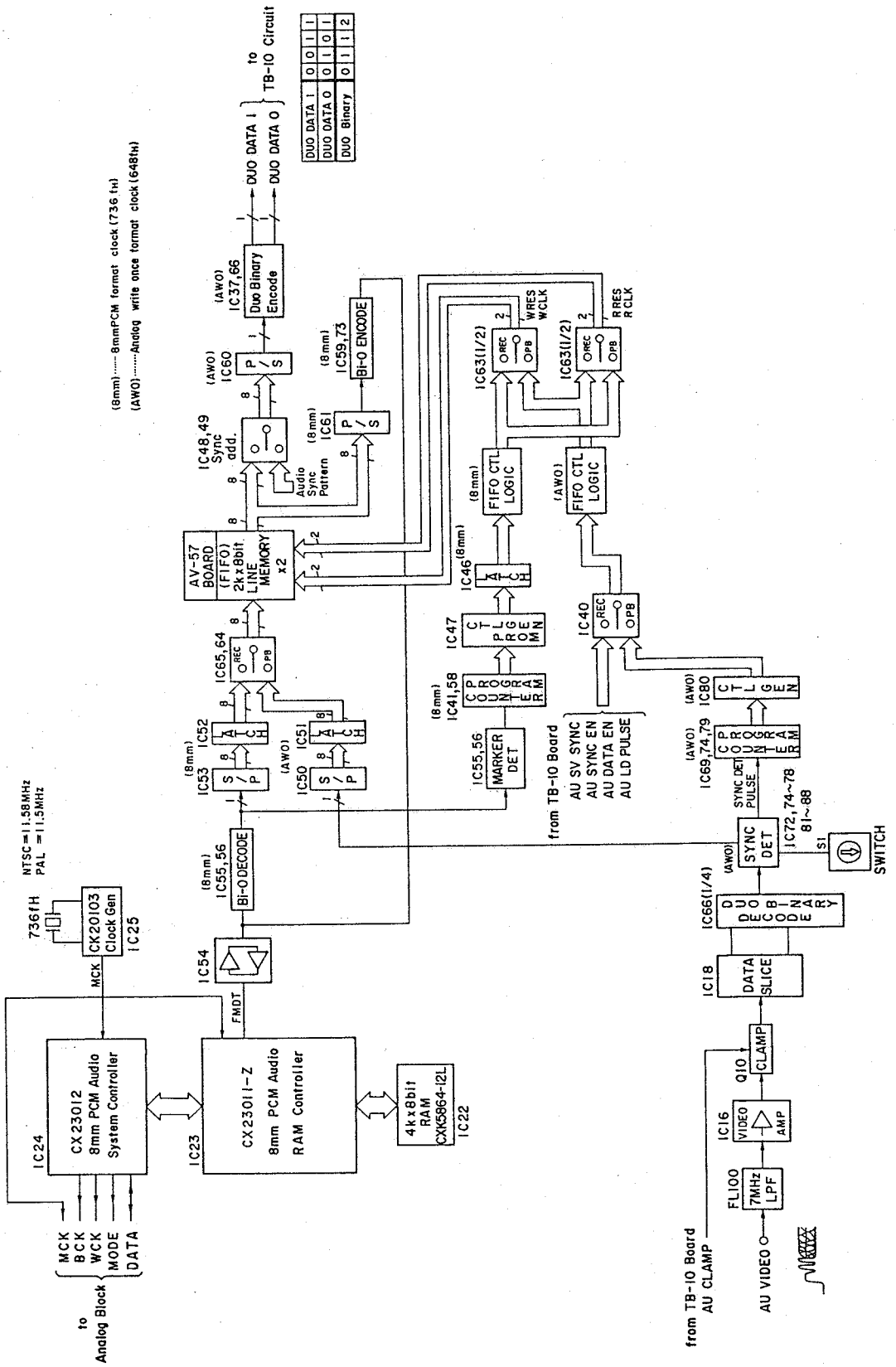


Fig. 4-7 Digital audio block diagram

4-2-3 RECORDING SYSTEM CIRCUIT

(1) 10-8 bit conversion circuit (See Figs. 4-8 and 4-9.)

The 10-bit serial data that is sent from the A/D converter is input to pin (16) of IC24. For signal processing, this IC performs 10-8 bit conversion and executes during playback the timing and control of the error's data interpolation and the PCM system.

Fig. 4-8 shows a block diagram of the internal section. The 10-bit data input from pin (16) undergoes 10-8 bit conversion. This is called non-linear quantization (bent line quantization). For recording, this compresses the data in order for the dynamic range to occupy a large portion on the tape's limited recording capacity. And for playback, the data is expanded back to its original state through demodulation. At high signal levels, the human ear can hardly hear noise since there is masking. Therefore, as shown by the conversion graph in Fig. 4-9, at low levels, the lower 8-bits of the 10-bit data are used as is. And as the level becomes higher, it becomes rougher from 9-bit, 8-bit, to 7-bit. This allows the dynamic range to occupy an equivalent of 10-bits despite the 8-bit recording capacity. The 8-bit data that has been converted is output from pin (9) . The clock for data transfer is pin (4) TCK.

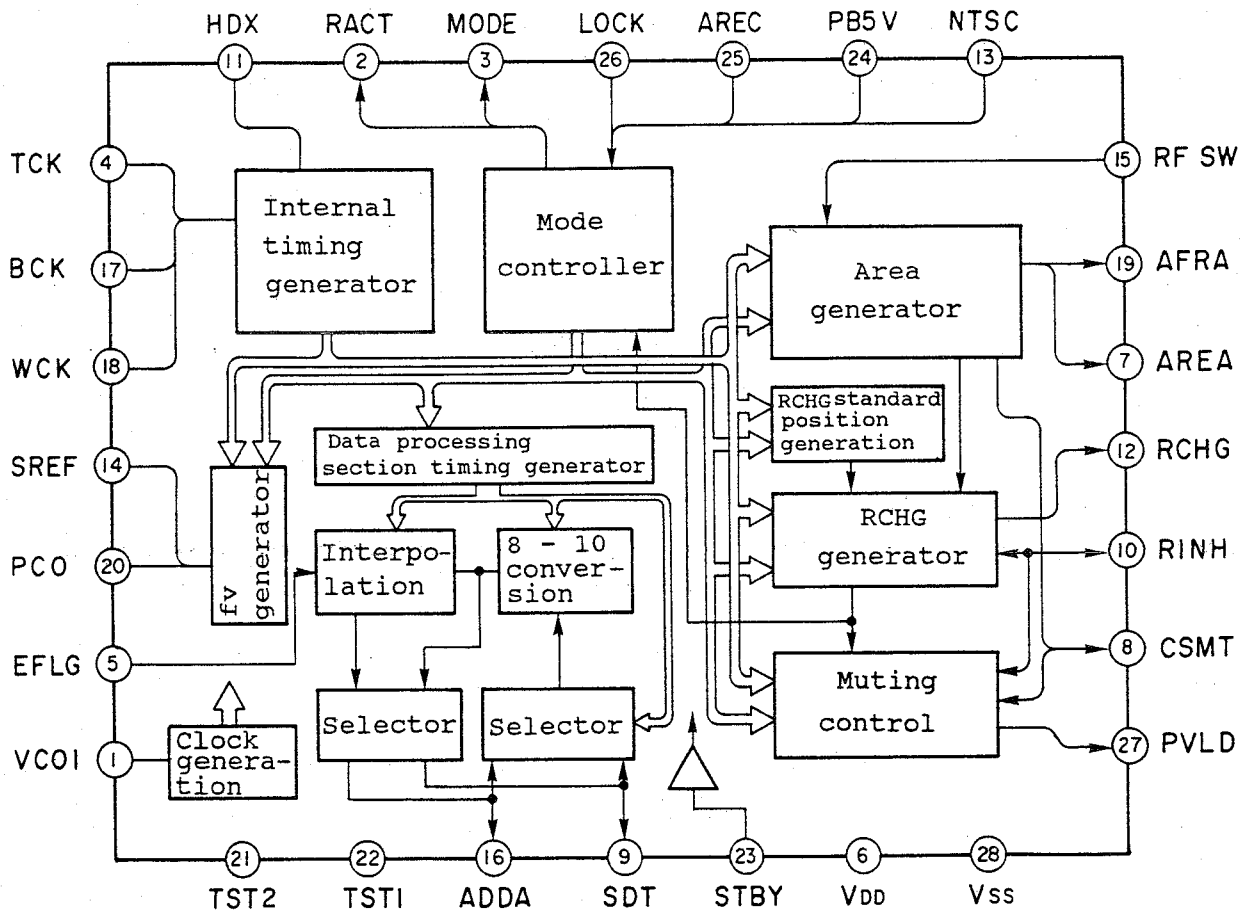
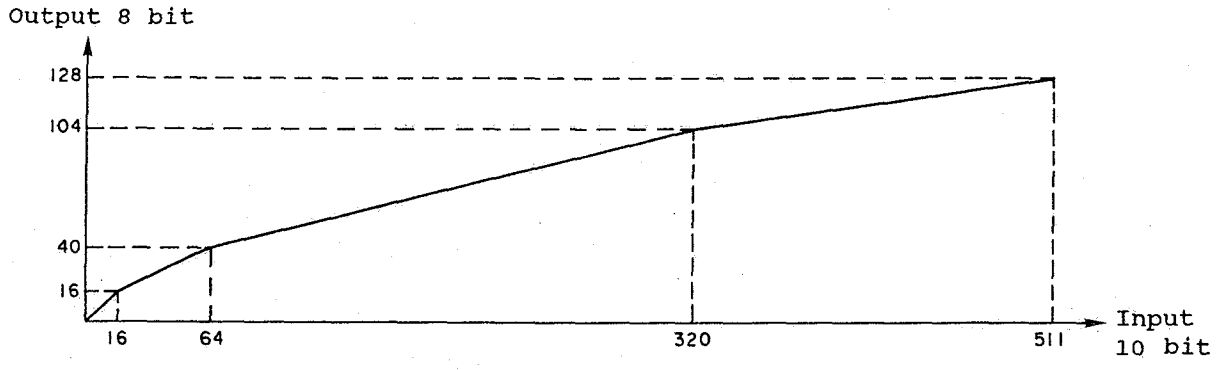


Fig. 4-8 Block diagram of IC24 (CX23012)



(a) 10 - 8 bit conversion graph

Y = X	(0≦X≦ 16)
Y= 〔X／2〕+8	(16≦X≦ 64)
Y= 〔X／4〕+24	(64≦X≦320)
Y= 〔X／8〕+64	(320≦X≦511)

X : Input absolute value (Input absolute value)
Y : Output absolute value(Output absolute value)

(b) Conversion algorithm

Encode formula	Input data	Output data
10bits→10bits	0 — 15	0 — 15
10bits→ 9bits	16 — 63	16 — 39
10bits→ 8bits	64 — 319	40 — 103
10bits→ 7bits	320 — 511	104 — 127

Fig. 4-9

(2) Cross interleave and CRCC (See Fig. 4-10.)

The 8-bit data output from IC24 is input to pin (40) of IC23. This IC operates for error correction. The 8-bit serial data is taken in by IC23 by the transfer clock TCK's (pin (45)) last transition. Then it undergoes serial/parallel conversion by the data interleave block and passses through the port controller block. It is then written onto the 32 Kbit RAM (IC22).

When the writing of one field of data is completed, the cross interleave code's encoding operation begins. For the encoding, the cross interleave block follows the procedure determined by the 8mm VTR PCM format, and RAM is accessed via the port controller. Then the data is taken from RAM. At the same time, the two codes of P parity and Q parity are added, then the data is sent to the CRCC (Cyclic Redundancy Check Code: code for detecting errors) block. The data undergoes parallel/serial conversion in the CRCC block, and CRCC is generated. Then the data is added with an error correction code (generating function) and undergoes FM modulation (Bi-phase mark) in the FM modulation block. The data's 0 becomes 2.9 MHz and 1 becomes 5.8 MHz. The data is output from pin (2).

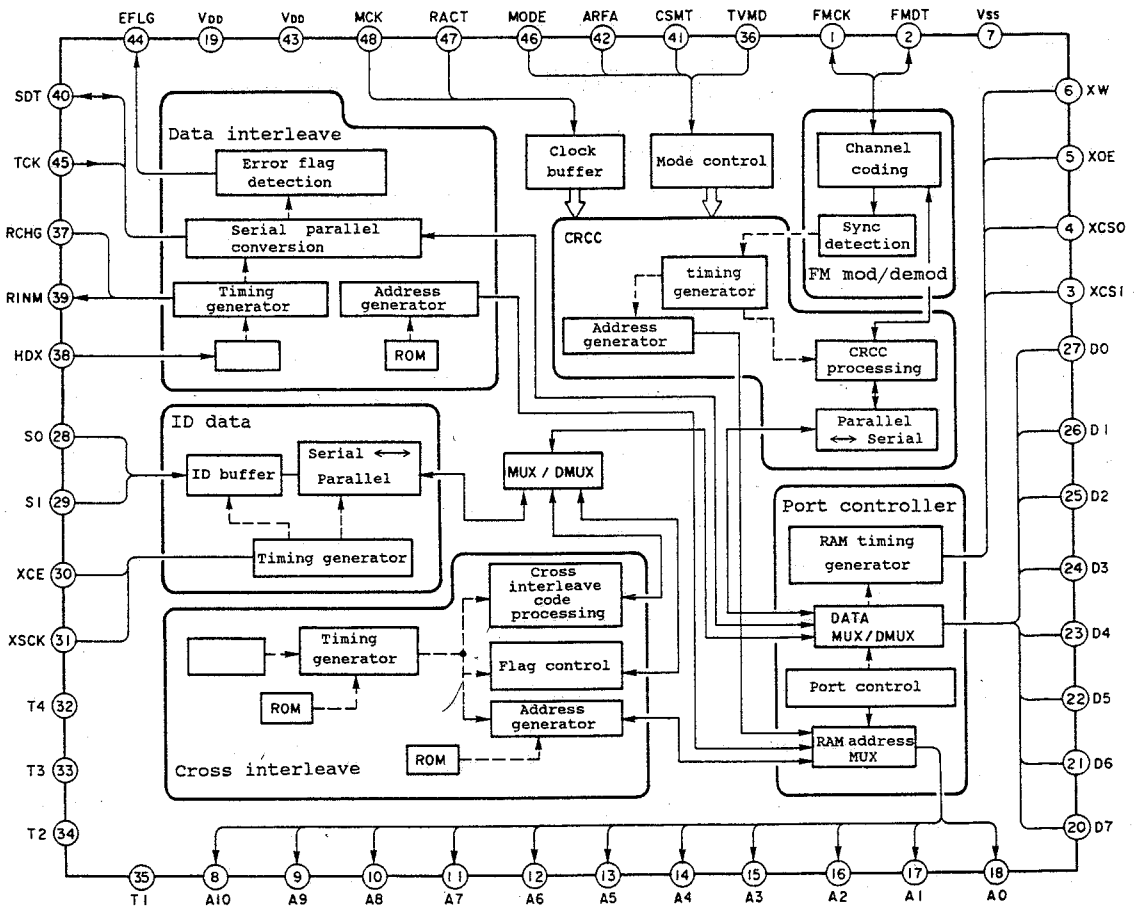


Fig. 4-10 Block diagram of IC23 (CX23011)

(3) 736 fH clock generator (See Fig. 4-11.)

IC25 (CX20103) is a master clock generator synchronized with the 8mm PCM system. the 8mm PCM system uses as the standard, a standard signal called SREF which has 1 field synchronization. This SREF and the master clock MCK have to be phase locked. Consequently, to enable phase comparison in IC24 (CX23012), MCK is input from pin (1) of IC24 and SREF is input from pin (14). Phase comparison is then performed. Comparison result PCO is output from pin (20) and taken in by pin (14) of IC25. PLL is then activated and VCO is controlled. MCK is then phase locked with SREF.

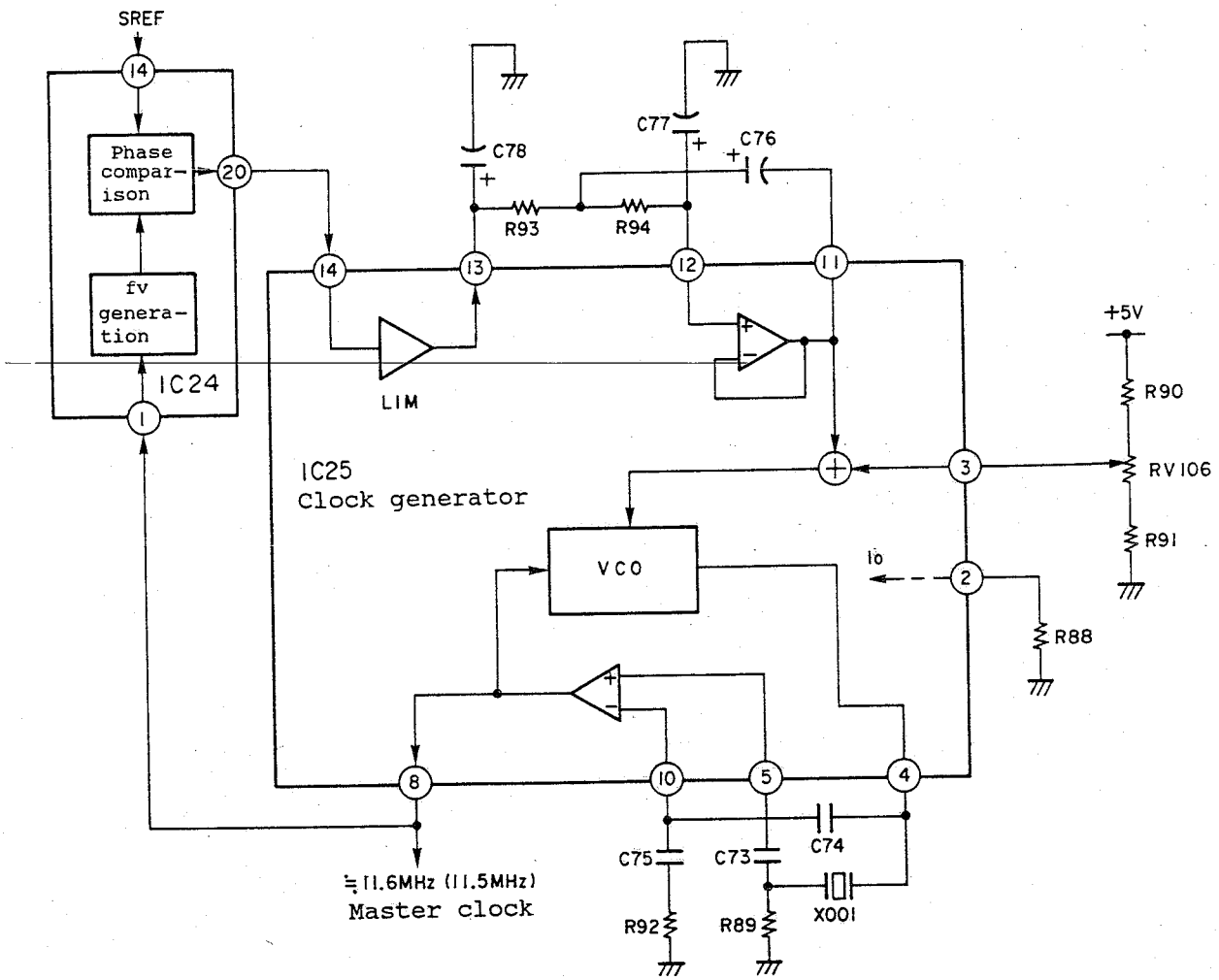


Fig. 4-11 IC25 (clock generator)

(4) Bi-Ø demodulation and parallel data conversion

The FMDT signal that is output from pin (2) of IC23 undergoes Bi-Ø modulation. Therefore EXOR is taken by IC066, and NRZ's information is extracted. Also, for this FMDT, there is a marker between the data that has undergone Bi-Ø modulation. The pattern is extracted by IC056, and the $\overline{\text{MARKER DET}}$ signal is output. This signal is in pin (1) of IC41 and IC58, and it is the standard signal for outputting the FMDT signal's incorporation timing after Bi-Ø demodulation.

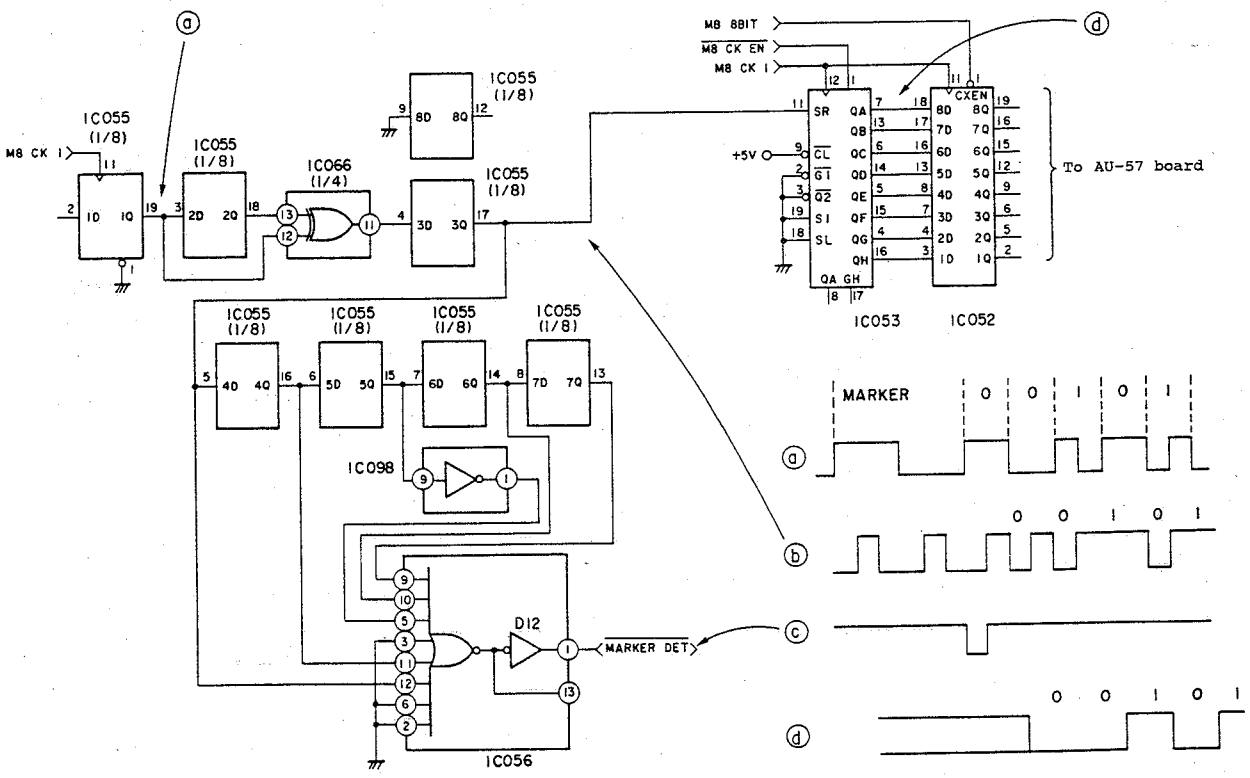


Fig. 4-12 Bi-Ø demodulation and marker detection circuits

In addition, the FMDT after Bi-Ø demodulation is input to pin (11) of IC053. As shown in Fig. 4-12 (d), after FMDT is fetched as NRZ's waveform, it is latched (IC052) in 8-bit units and converted into parallel data.

After the conversion, FMDT is given to the AU-57 board for conversion to the analog WO format.

(5) Audio frame memory (See Fig. 4-13.)

During recording, this board operates to convert the 8-bit parallel data that was input in the 8mm format, into the 8-bit analog WO format. The board then outputs the data. During playback, the data is converted in reverse, from the analog WO format into the 8mm format.

This board has two audio field memories: IC708 and IC709. While one memory undergoes a writing operation, the other memory undergoes a reading operation. The two memories changeover between these two operations for each field.

Also, by having the standard signal for the 8mm PCM system operate SREF, the audio signal's sampling starting position is matched to the video signal's V blanking interval.

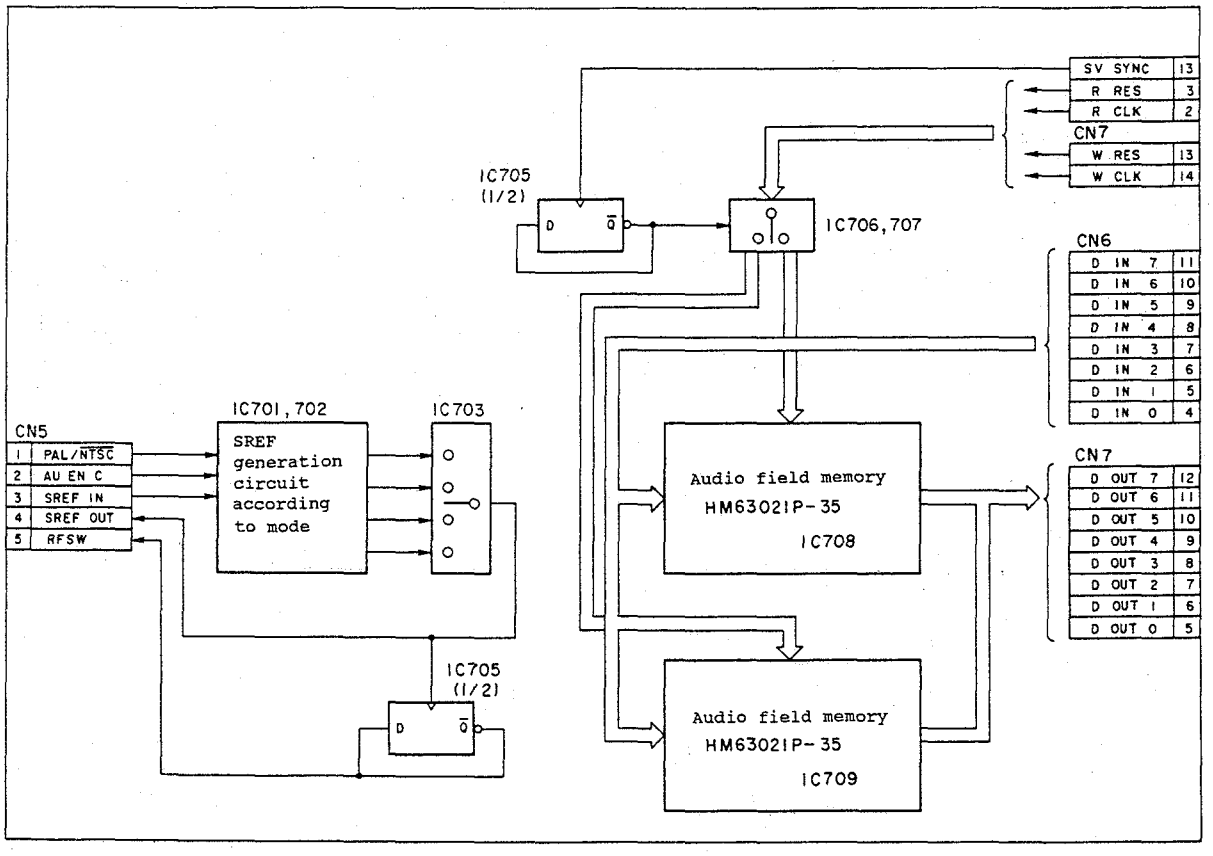


Fig. 4-13 Block diagram of the AU-57 board

(6) Audio SYNC added circuit and duo-binary modulation (See Fig. 4-14.)

The data that has been converted into the analog WO format enters IC48 and IC49's selector. After being added with a sync pattern called "00100111", the data is sent to IC60, which is a parallel → serial converter. After the data becomes a serial data, it is input to pin (10) of IC066, and duo-binary modulation is performed.

Fig. 4-14 shows the duo-binary condition of the above audio SYNC pattern which is included in one location above the video signal line 1. In the figure, (a) is the serial audio data that is input, (b) is the pulse that resets the duo-binary modulation, and (c) and (d) are two audio signals that are output to the TB-10 board. On the TB-10 board. On the TB-10 board, the (c) and (d) waveforms are mixed, and the waveform shown in the figure is loaded onto the analog WO's time sharing video signal. (Since it actually passes through a limited band filter, the waveform looks like a sine wave.)

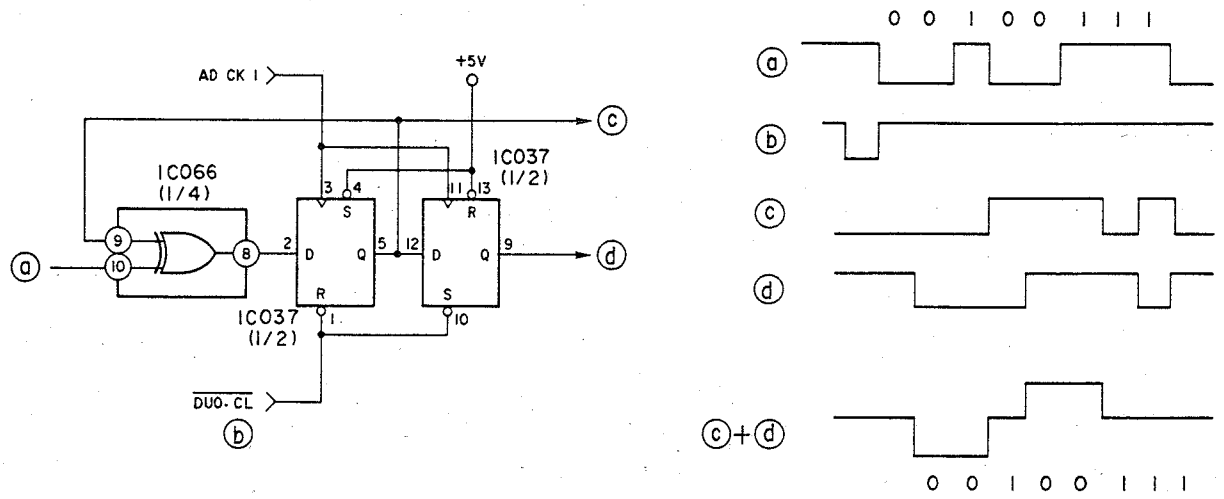


Fig. 4-14 Duo-binary modulation

4-2-4 PLAYBACK SYSTEM CIRCUIT

(1) Clamp circuit and data slice circuit (See Fig. 4-15.)

The analog WO format signal (hereinafter, AU VIDEO signal) played back from the disc passes through the 7 MHz LPF (FL100) and enters pin (4) of video amplifier IC16 (VA). It is then amplified by about 12 dB and clamped by Q010 (2SK363) so that the pedestal level becomes GND. RV109 is adjusted so that it becomes 1 V between the pedestal of the clamped AU VIDEO signal and the audio signal's center level. (See Fig. 4-14.)

The clamped AU VIDEO signal is input to comparator IC18 (SN75107) and sliced at two locations of the audio signal eye's cross points (C1) and (C2) in the figure). The signal then becomes two lines of digital data which are output from pin (4) and (9) of IC18. (C1) is adjusted by RV001 and (C2) is adjusted by RV002.

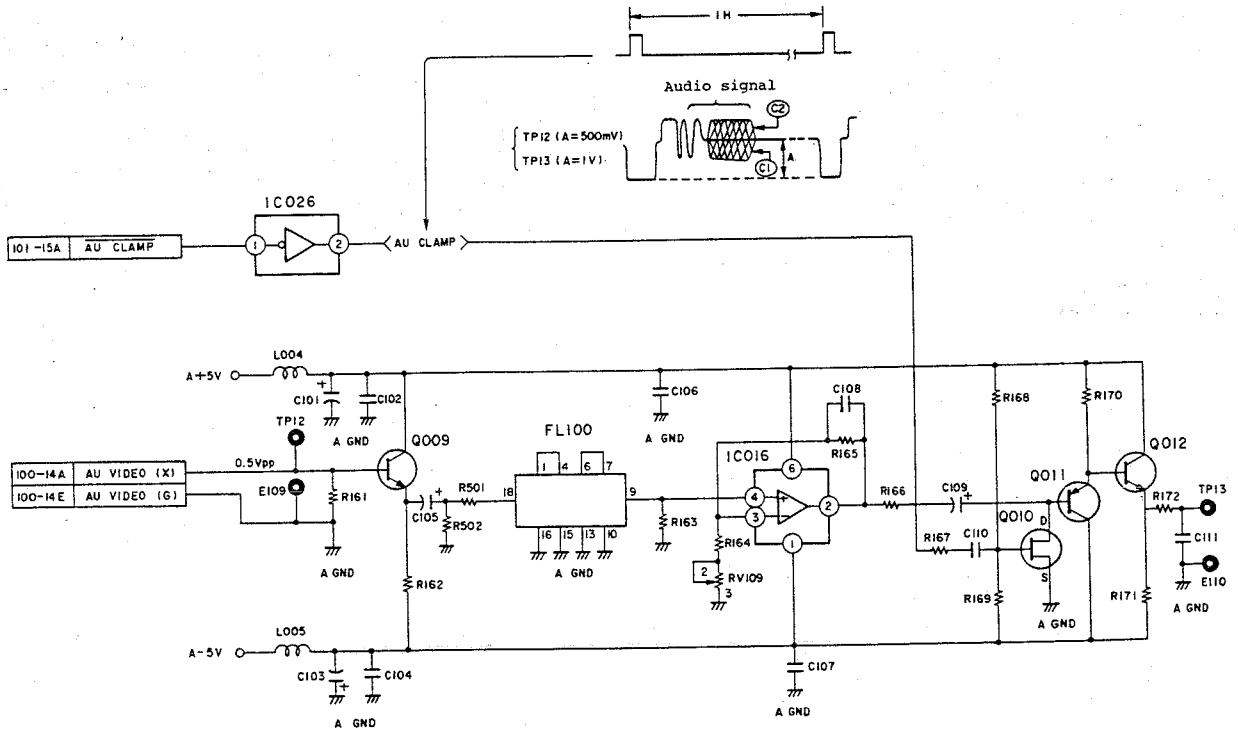


Fig. 4-15 AU VIDEO input step

(2) Duo-binary demodulation circuit

The two lines of audio data that are compared by IC18 enters pins (4) and (5) of IC066, then duo-binary demodulation is performed. Fig. 4-15 shows the demodulation of the audio SYNC pattern. Since the demodulated data is converted from 3 values to 2 values, it is output from a single pin, pin (6).

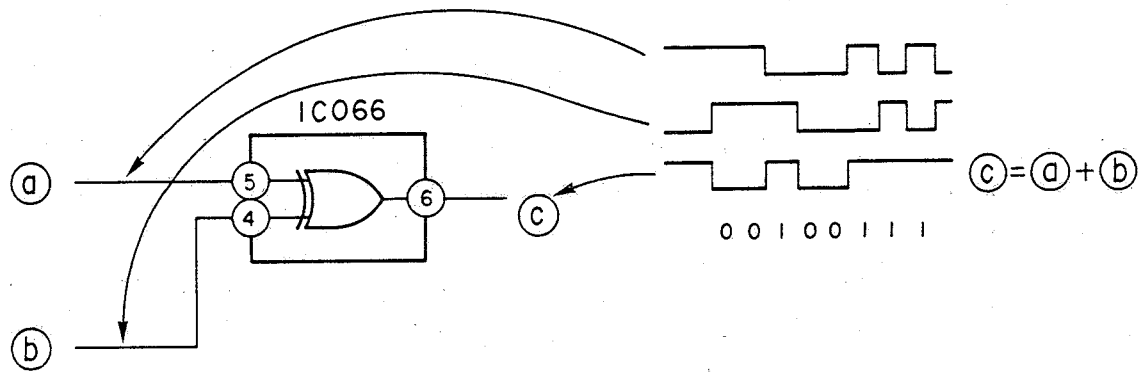


Fig. 4-16 Duo-binary demodulation

(3) Audio SYNC detection circuit and control circuit

The demodulated data that is output from pin (6) of IC66 is input to pin (1) of the delay-line IC74 (ZT35-100). This is to select its optimum phase with the 648 fH master clock ADCK which is sent from the TB-10 board. After passing through delay line, the signal is first output to pin (2), then to pins (5), (13), and (11) with a time difference of 20 ns for each pin. Each output enters the respective shift resistors IC78, IC77, IC75, and IC76. The audio SYNC patterns are detected by the respective comparators IC88, IC87, IC85, and IC86. The SYNC detection pulse is output from pin (19) of the comparator IC and input to IC82. In IC82, only when $\overline{\text{PB SYNC EN}}$ that is being input to pin (19) is in interval "L," the four SUNC detection pulses are looked at, and the selection of the four lines of time-different audio data is determined in correspondence to the rotary switch S1's lower 2 bits of information. Then the select signal is sent to pins (2) and (14) of IC82's selector. Also, the SYNC detection pulse is sent to the control signal generator circuit's counter IC. Table 4-1 shows the relationship between the S1's lower 2 bits and IC72's select signal.

Table 4-1 Data selection by rotary switch S1

Rotary switch S1 value	Selector IC72		Delay amount for the selected data
	Pin ②	Pin ⑭	
0, 4, 8, C	L	L	No delay (To be the standard)
1, 5, 9, D	L	H	+20ns delay
2, 6, A, E	H	L	+40ns delay
3, 7, B, F	H	H	+60ns delay

The SYNC detection pulse is output from pin ⑨ of IC82. And after it is clocked by IC81, it enters the playback analog WO format control generation circuit. Counter IC70, IC69, and IC79 of this circuit operate at 1H periods. The SYNC detection pulse is used as their reset signal. Even if the SYNC detection pulse is missing due to an error, this counter itself will interpolate the detection pulse and count properly. This interpolation pulse is output from pin ⑲ of IC80, then it takes the OR of the true detection pulse.

Also, this counter receives the status information for the H unit, called AU EN1 and AU EN2, from the TB-10 board. The value loaded to the counter is changed, and each control signal also changes according to the changes of the count value. Table 4-2 shows AU EN1 and AU EN2 and the quantity of audio data that is included in them. According to this table, when there are the PB LD PULSE and the audio data that has 8-bit partitioning, the PB DATA EN that becomes active is output from pins ㉒ and ㉑ of IC80. Also, these two signals are "L" active.

Table 4-2 Polarity of AU EN and quantity of audio data

AU EN2	AU EN1	Quantity of audio data within 1 H		Quantity of lines within 1 field	
		PAL	NTSC	PAL	NTSC
0	0	5 bytes	5 bytes	284 lines	236 lines
0	1	69 bytes	67 bytes	9 lines	8 lines
1	0	0 byte	0 byte	——	——
1	1	0 byte	0 byte	——	——

After SYNC detection, the audio data enters shift resistor IC50 as PB DATA and becomes 8-bit parallel data to enable its entry to the memory on the AU-57 board. When the $\overline{\text{DATA LD}}$ pulse that is being input to pin ① of IC51 is "L", the output data from IC50 is latched. Then after passing through selector IC64 and IC65, the pulse is sent to the AU-57 board.

In accordance with the analog WO format, the audio data that has been dispersed to each H

passes through the AU-57 board for conversion into the 8mm PCM format. The data after the conversion is input to the parallel → serial converter IC61. The serial output is obtained from pin (13).

(4) Bi-Ø modulation

The serial data that has been converted to the 8mm PCM format is output from pin (13) of IC061. However, since it is still the data for NRZ, Bi-Ø modulation must be performed before the data is input to LSI IC23. IC073 and IC059 are used for Bi-Ø modulation. From the output of pin (13) of IC61, a 01 repeat signal, called Bi-Ø ENC, or OR and NOR are taken and input to pins (2) and (3) of IC059. IC059 executes toggle operation when pin (2) is "H" and pin (3) is "L". Therefore when the audio data is "L", there is one toggle for one bit. When it is "H", two toggle operations will obtain Bi-Ø modulation. Also, a marker is added when the Bi-Ø ENC signal is operated, and there are two toggle operations for 3 bits.

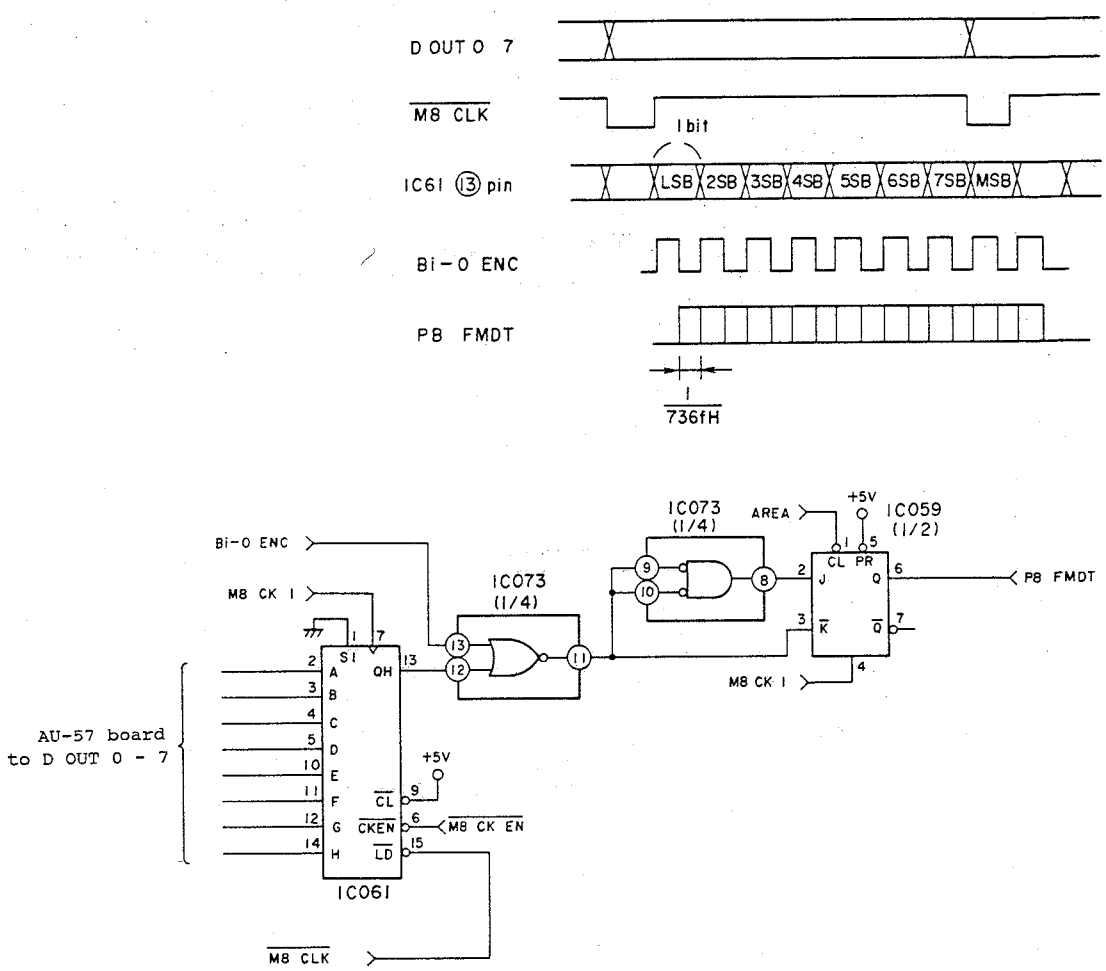


Fig. 4-17 Bi-Ø modulation

(5) De-interleave and error correction

The PB FMDT signal that is output from pin (6) of IC59 passes through the tristate buffer IC54, then it is sent to pin (2) of IC23. Then it undergoes Bi-Ø demodulation in the LSI. Next, error detection is performed in the CRCC block of IC23. If no error is detected, the data undergoes serial-parallel conversion and passes through the port controller block. Then it is written to RAM (IC22). The cross interleave code is then decoded. If there is an error, it is corrected. After the decoding is completed, the data undergoes parallel-serial conversion in the det-interleave block, then it is output from pin (40) as serial data.

(6) 8-10 conversion and dat interpolation

The 8-bit serial data that is output from pin (40) of IC23 is input to pin (9) of IC24 and converted to 10-bit. Then it is output from pin (16). However, if there are more errors than IC23 can correct, EFLG (error flag) of pin (44) of IC23 becomes "H". Without IC23 performing error correction, the data is interpolated (primary and secondary interpolations) by IC24. Also, if there are more errors than can be interpolated, the data is substituted (Prehold) with the immediately-preceding field data. If this continues for four or more fields, muting is done.

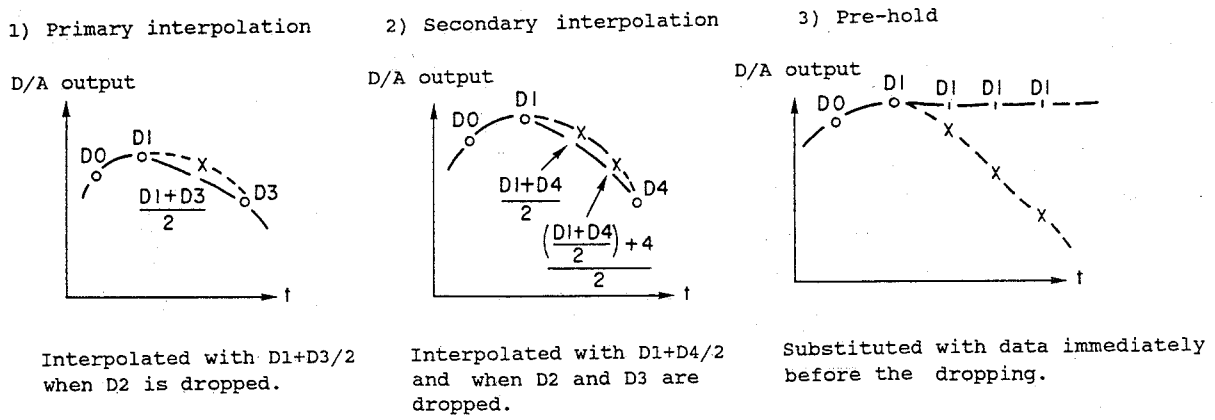


Fig. 4-18 Interpolation system